Université du Québec
Institut National de la Recherche Scientifique
Centre Énergie Matériaux Télécommunications

Sinter-free fully inkjet-printed flexible valency change memory

Par
Mohamed Delfag

Thèse présentée pour l'obtention du grade de
Philosophiae Doctor (Ph.D.)
en sciences de l'énergie et des matériaux

Jury d'évaluation

Président du jury et Examinateur interne	Professeur Shuhui Sun Institut National de la Recherche Scientifique Centre Énergie Matériaux Télécommunications
Examinateur externe	Professeur Fabian Ezema University of Nigeria, Nsukka Department of Physics and Astronomy
Examinateur interne	Professeur Rafik Naccache Université Concordia, Montréal Chemistry and Biochemistry
Directeur de Recherche	Professeur Andreas Ruediger Institut National de la Recherche Scientifique Centre Énergie Matériaux Télécommunications
Codirecteur de recherche	Professeur Christina Schindler Munich University of Applied Sciences Department of Applied Sciences and Mechatronics

ACKNOWLEDGEMENTS

First and foremost, I want to express my gratitude to my wife and kids for their understanding and being patient with me during the numerous busy days I spent working on my research. I would like to express my gratitude to my supervisor Prof. Andreas Ruediger and my co-supervisor Prof. Christina Schindler. They provided me with the opportunity to work in the fascinating topic of printed resistive memory as part of their successful collaboration.

Prof. Andreas Ruediger, who diligently supported me from the very beginning of my studies. His permanent support, encouragement as well as his constant availability for an exchange of ideas were essential for the completion of my work. His welcoming, collegial, and considerate attitude without the slightest reservation will always remain with me as a unique inspiration.

I am grateful to Prof. Christina Schindler for her unwavering assistance and her always open door in Munich.

The Nanophotonics team has fostered a fun and productive working atmosphere. I would especially want to thank Dr. Yoandris Gonzalez, Giorgos Rachovitis, and Dr. Johannes Jehn for helping me with my experimental work, as well as Dr. Rajesh Katoch, Dr. Andreas Dörfler Dr. Ifeanyichukwu Amaechi, Dr. Azza Youssef for their scientific expertise. Last but not least, I would like to express my gratitude to Mr. Anouir Hamdi for his assistance with the French translation.

ABSTRACT

Additive manufacturing provides a highly competitive platform for rapid prototyping, small volume production and point-of-use production and has expanded to printable electronics over recent decades. While the impact in display technology and more recently in the production of photovoltaics has been transformative for the respective industries, other electronic components for logic and in particular memory are still in their infancy.

In this respect, resistive random access memory is particularly attractive to the printing process due to its simple three-layer structure. Recent progress with fully printed conductive bridge memory cells demonstrated the feasibility of the approach and yet, it relied on a process including three different materials and multiple sintering steps. Here, we suggest a sintering free fabrication with only two different materials. The respective memory cells consist of symmetric electrodes of PEDOT:PSS and an insulating layer of either ZnO or WO_3 on transparent, flexible PEN substrates. Based on the choice of the materials, the underlying mechanism causing the resistance change of the cell under bias voltage is demonstrated to be according to “valency change” microscopic origins.

The logical state ("0" or "1") of this memory cell is determined by its resistance measured between both electrodes. The current conduction in the ON state is determined by localized filamentary features, space charge limited in the high resistance state, facilitated through the migration of oxygen vacancies, at low voltages (< 2V) and Schottky emission dominates the current conduction for higher voltages (>2V) across the interface between the PEDOT: PSS electrode and dielectric WO_3. The cells show good retentivity and endurance (> 6000 cycles).

Conductive atomic force microscopy provided direct microscopic evidence that the switching for the PEDOT:PSS/ZnO/PEDOT:PSS printed devices relies on the development and dissolution of an oxygen vacancy filament. While the space charge limited conduction (SCLC) mechanism was said to be the conduction mechanism for the high resistance state (HRS). Memory cell switching,

endurance, and retention characteristics were examined, and the results showed that the HRS and low resistance state (LRS) are stable for more than 10^4 cycles and 10^5 s, equivalent to ZnO-based ReRAM produced by clean-room methods.

Both materials provide devices with very good optical transparency in the visible range. Bending experiments for ReRAM cells based on both materials demonstrate stable operation for up to 700 cycles down to bending radii of approximately 3 mm and a failure mechanism induced by the electrode material rather than the resistively switching layer. The cells are entirely sinter free and no electroforming is required to activate them. These characteristics make them suitable for the next generation of flexible non-volatile memory devices.

Keywords:
Printed electronics, flexible electronics, resistive switching, printed memory

RÉSUMÉ

La fabrication additive offre une plateforme très compétitive pour le prototypage rapide, la production en petites séries et la production au point d'utilisation. Au cours des dernières décennies, elle s'est étendue à l'électronique imprimable. Alors que l'impact dans la technologie des écrans et plus récemment dans la production de photovoltaïques a été transformateur pour les industries respectives, d'autres composants électroniques pour la logique et en particulier la mémoire en sont encore à leurs débuts.

À cet égard, la mémoire vive résistive est particulièrement intéressante pour le processus d'impression en raison de sa structure simple à trois couches. Les progrès récents réalisés avec des cellules de mémoire à pont conducteur entièrement imprimées ont démontré la faisabilité de l'approche, mais ils reposaient sur un processus comprenant trois matériaux différents et de multiples étapes de frittage. Nous proposons ici une fabrication sans frittage avec seulement deux matériaux différents. Les cellules de mémoire respectives sont constituées d'électrodes symétriques en PEDOT:PSS et d'une couche isolante en ZnO ou WO_3 sur des substrats transparents et flexibles en PEN. Sur la base du choix des matériaux, il a été démontré que le mécanisme sous-jacent à l'origine du changement de résistance de la cellule sous une tension de polarisation était dû à des origines microscopiques de "changement de valence".

L'état logique ("0" ou "1") de ces cellules mémoire est déterminé par sa résistance mesurée entre les deux électrodes. La conduction du courant à l'état ON est déterminée par des caractéristiques filamentaires localisées, une charge d'espace limitée dans l'état de haute résistance, facilitée par la migration des lacunes d'oxygène, à de faibles tensions (< 2V) et l'émission Schottky domine la conduction du courant pour des tensions plus élevées (>2V) à travers l'interface entre l'électrode PEDOT : PSS et le diélectrique WO_3. Les cellules présentent une bonne rémanence et une bonne endurance (> 6000 cycles).

La microscopie à force atomique conductrice a fourni une preuve microscopique directe que la commutation des dispositifs imprimés PEDOT:PSS/ZnO/PEDOT:PSS repose sur le développement et la dissolution d'un filament de vacance d'oxygène. Alors que le mécanisme de conduction limitée par la charge d'espace (SCLC) était considéré comme le mécanisme de conduction pour l'état de haute résistance (HRS). Les caractéristiques de commutation, d'endurance et de rétention des cellules de mémoire ont été examinées, et les résultats ont montré que le HRS et l'état de faible résistance (LRS) sont stables pendant plus de 10^4 cycles et 10^5 s, ce qui équivaut à la ReRAM à base de ZnO produite par des méthodes de salle blanche.

Les deux matériaux fournissent des dispositifs avec une très bonne transparence optique dans le domaine visible. Les expériences de flexion pour les cellules ReRAM basées sur les deux matériaux démontrent un fonctionnement stable jusqu'à 700 cycles jusqu'à des rayons de flexion d'environ 3 mm et un mécanisme de défaillance induit par le matériau de l'électrode plutôt que par la couche à commutation résistive. Les cellules sont entièrement exemptes de frittage et aucun électroformage n'est nécessaire pour les activer. Ces caractéristiques les destinent à la prochaine génération de dispositifs de mémoire non volatile flexibles.

TABLE OF CONTENTS

LIST OF FIGURES

List of Tables

List of Abbreviations

AFM	Atomic Force Microscopy
CAFM	Conductive Atomic Force Microscopy
CMOS	Complementary Metal-Oxide Semiconductor
DRAM	Dynamic Random Access Memory
ECM	Electrochemical Metallization Memory
FeFET	Ferroelectric Field Effect Transistor
FeRAM	Ferroelectric Random Access Memory
FTJ	Ferroelectric Tunnel Junction
HRS	High Resistive State
LRS	Low Resistive State
MRAM	Magnetic Random Access Memory
PCM	Phase Change Memory
PEDOT:PSS	poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
PEN	poly(ethylene 2,6-naphthalate)
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
SRAM	Static Random Access Memory
STT-RAM	Spin-Transfer Torque Random Access Memory
VCM	Valence Change Memory

CHAPTER 1

1 INTRODUCTION

New applications in information and communication technologies, such as video, multimedia entertainment, and data/information services, keep penetrating the consumer market with increasing performance, complexity, and abundance. Especially in the area of Internet of Things (IoT), where a large amount of interconnected devices are used to add “smart“ qualities to products, a trend that is predicted to increase quickly over the coming years [1]. All these new applications require storage of data, most of which is small enough to be locally stored.

While Flash memory can store a large amount of data [2][3], its manufacturing comes with a very large technological effort and economy of scale, such that custom circuit integration for small series is economically unviable. The exact opposite is true for printed electronics: There is little overhead for small or custom series production. Additionally, the printed electronics can easily be attached to everyday products, with functionalities specific to the product. The envisioned aim of these memory devices is that they can be produced with very low technological requirements, just like standard inkjet printing, and retain data without power. Besides the non-volatility, these devices competitiveness depends less on capacity and write/read access times rather than on complementary characteristics such as low power consumption, flexibility and optical transparency [4].

Despite some of the benefits of classical CMOS technology, there are various applications that call for functionalities such as flexibility and optical transparency albeit at the detriment of storage capacity. The need for advanced clean-room facilities for the production of the aforementioned transistor-based devices is incompatible with point-of-use production where relatively moderate memory capacity is acceptable. Possible examples are multi-use tickets for

public transport that carry information about the types of fares booked, smart tags that track e.g. temperature or other external parameters during transportation, or the stored items in a warehouse: The list keeps evolving as the opportunities for point-of-use production evolve. A technique that we all became acquainted with to produce high quality documents and photos without need for a dedicated press, is printing. While the early needle-printers were soon replaced by ink-jet or laser printers, the freedom to produce high quality documents any time is still a pillar of office management around the world.

What, if this freedom to produce high quality, relatively low quantity units could be extended from documents to electronic circuitry with the respective functionalities? This has already been realized to a large extent for displays, and there is an increasing demand to push these complementary components of electronic circuitry including logic and memory towards the market. From 2018 to 2025, the global printed electronics market is predicted to grow at a compound annual growth rate of more than 11 percent, reaching USD 17.26 billion. The market's significant trends include increased Internet of Things penetration, the evolution of digital print technology, reduced production costs, need for durable and flexible substrates for generating secure printed electronics, and eco-friendly technologies [5].

1.1 Recent developments and State of the Art

Printed electronics already possess the necessary technological maturity to manufacture most of the required components using printing techniques. On transparent, thin substrates with extremely precise sizes and designs suitable with crossbar memory architecture, inkjet printing has been successfully used and even demonstrated sinter-free process flows with electrodes and dielectric materials [6]. There have already been printed sensors for acquiring pressure, strain, temperature, humidity, and more [7]. A contactless data transfer can be achieved with printed Radio-Frequency (RF) identification tags [8]. Moreover, power supply to embedded systems can

be provided by printed batteries [9]. Additional circuit elements, such as a resistor, capacitor, and inductor can be printed to form fully printed electronic circuits.

Since 1994, printed transistors have been demonstrated; and today, fully printed diodes operating at frequencies up to 1.6 GHz are available [10]. Today, every single circuit element including the memory unit is printable to evolve towards fully printed circuits. In particular, for the case of memory applications, printing is suitable in the fabrication of Resistive Random Access Memory (ReRAM) since it only requires of a relatively simple metal-insulator-metal (MIM) structure with a minimum cell size of $4F^2$, where F is the minimum feature size determined by the manufacturing process.

The field of printed electronics, because of its high growth rate, is characterized by constant change and fast evolution. Up to now, printed electronic devices almost exclusively used semiconductor chips as memory devices; however, directly printed memory has shown significant improvements. Organic materials have been used to print flash memory, which is the most widely used memory based on semiconductor chips [11]. However, in a self-sustaining system, the switching voltage of up to 50 V is too high to be operated by batteries. There have not been any reports of printed Phase change memory (PCM), magnetic RAM (MRAM).

To enable binary logic, the fundamental memory unit of any new memory technology, also called a memory cell, must be switchable between at least the two logic states "0" and "1". The logic states are defined by the resistance of the memory cell: a high resistance state (HRS) corresponds to "0" and a low resistance state (LRS) corresponds to "1". "Resistive RAM" is a descriptive name since logic states are determined by the resistance of the memory cell.

Not all these technologies are readily transferred to printed circuitry: The phase change material combination Ge, Sb, and Te remains difficult to print for PCM. MRAM and STT-RAM rely on a thin tunnel barrier in the nanometer range for their performance, which is extremely challenging

difficult to create by printing technology [12]. The same is true for ferroelectric tunnel junctions, which feature thin ferroelectric layers. While it is possible to reach the required low thicknesses through spin-coating, no printed FTJs have so far been reported. FeRAM structures may be printed using ferroelectric polymers. To prevent electrode short-circuits, their printed ferroelectric layer must be thicker than evaporated layers. As a result, printed FeRAM experiences high switching voltages of around 20 V [13].

Conductive bridge and valency change ReRAM is particularly appealing for printing because of its simple three-layered construction combined with potentially low operating voltages. This has resulted in an increase in the number of publications on printed ReRAM devices in recent years. Different architectures and material combinations are studied, as well as combinations of different printing technologies and partially printed cells.

Zou et al. reported in 2014 on a bipolar Ag/Cu/CuxO/Ag ReRAM with printed Ag layers and electroplated Cu [14]. The switching capabilities and flexibility of the cells were intriguing, but the electroplating stage remained a time-consuming and disruptive part of the manufacturing process. Vilmi et al. presented an inkjet-printed Ag/TiOx/Ag memory cell in 2016 that was already coupled to a piezoelectric transducer to form a self-sustaining device [15]. This ingenious combination of a memory cell and an energy harvesting sensor was extremely innovative. Its manufacture, however, requires an additional lithography process, and the cell is only capable of a few switching cycles before failing. In 2017, Vescio et al. presented their results on Au/HfO_2/Ag ReRAM cells using inkjet printer HfO_2 and Ag layers but sputtering for the Au bottom electrode [16].

The Choi group at Jeju National University has consistently reported fully printed ReRAM cells using electrohydrodynamic printing, which focuses on unipolar Ag/insulator/Ag architectures [17]. Although the more sophisticated approach of electrohydrodynamic printing can yield greater print resolution, it can be difficult to apply in a high throughput industrial process [18].

Nau et al. announced in 2015 the first fully inkjet-printed ReRAM, an Ag/poly(methyl methacrylate)/Ag structure. Select diodes have already been used to link single pole cells to form a 5x5 crossbar [19]. As a first feasibility test, this structure demonstrates that ReRAM cells can be fabricated solely by inkjet printing. The low yield, less than 20%, on the other hand, requires structural modifications or improvements in the printing process.

Within our own joint research among the groups at Munich University of Applied Sciences and INRS-EMT, previous PhD students were able to successfully demonstrate a fully printed conductive bridge RAM (sometimes also referred to as an electrochemical metallization cell) [20]. This device provided excellent performance under bending with the opportunity for optical transparency. More recently, our research groups demonstrated conductive bridge operation with copper electrodes.

1.2 Motivation

All these studies confirm the considerable interest in printed memory devices, and a tremendous potential towards applications. With cost-efficiency being one of the main driving forces of printable electronics [21], there are several remaining challenges that are almost universal throughout the industry and that are somewhat in analogy to the earlier developments in semiconductors [22]. To streamline the production process and to improve the lifetime of the components, different aspects of the printing process and of material sciences come into play:

1) The number of different inks that are required for a single device should be kept to an absolute minimum as every new ink requires a different print-head that calls for alignment, maintenance and that inevitably adds complexity to the process. Ideally, inks should be useable among different system components so that, electrode materials may serve for battery, memory, and logic alike.

2) The speed of the printing process, i.e., the transfer of ink to the substrate, is usually not the rate-limiting step in printed electronics. Almost all inks require the evaporation of the solvent before they develop their desired functionality and in the case of metal nanoparticle inks for electrodes as well as in the case of spin-on-glasses for dielectrics in conductive bridge memory, there is even a requirement of sintering to generate the desired properties. Sintering may be achieved in different ways with thermal sintering and photo-sintering being the most common ones. Thermal sintering is inexpensive but time-consuming, while photo-sintering may be fast but usually comes at considerable costs.

3) The chemical compatibility of inks and printed components can affect the printing process, as well as the device operation and lifetime. Inks have to meet different requirements that relate to the printability through the nozzles of the ink-jet printer (density, dynamic viscosity, surface tension), they should have an acceptable evaporation rate once printed but still low enough not to dry out and clog the nozzles during idle-times of the printer and as such and with all this in mind, they should remain sufficiently chemically inert in order to not react with any other component of the printing setup or other inks (unless desired).

4) The electrical and structural compatibility of components, mainly after the printing process is critical: Different thermal expansion coefficients, coffee-stain effects, evaporation rates and so on may give rise to cracks and other mechanical failure mechanisms while the electrical compatibility relates to the quality of contacts and their nature (Ohmic, Schottky-barrier or alike).

1.3 Research objectives and approach

Based on the aforementioned points, in particular with respect to the overall process speed, the key objective of this thesis is to demonstrate sinter-free, fully printed, flexible, and transparent memory cells.

This overall goal breaks down into the following sub-topics:

(i) to demonstrate a sintering-free printing of WO_3 or ZnO on flexible polyethylene naphthalate (PEN) substrates with symmetric PEDOT:PSS electrodes, thus only using two different inks each time

(ii) to identify and quantify the operation mechanism of the resistive memory cells. This is done with the aim of exploring the potential of printed valency change memory

(iii) to determine the endurance and retention of printed memory

(iv) to demonstrate operation under flexure

(v) to determine the optical transparency

(vi) to provide a quantified rationale about which material is better suited for valency change ReRAM

CHAPTER 2

2 FUNDAMENTALS

2.1 Types of Random Access Memory

Memories are major component in microelectronics. Its importance can be correlated with the development of portable electronics (cell phones, laptops, etc.), which requires ever greater storage capacities. The storage of information can be divided into two categories according to the type of memory, volatile or nonvolatile. Especially for mobile applications, where energy is scarce, non-volatile memory has the undeniable benefit of extending the operation time with a single battery charge. Volatile memories include several memory designs that in all cases require continuous power to maintain the stored information.

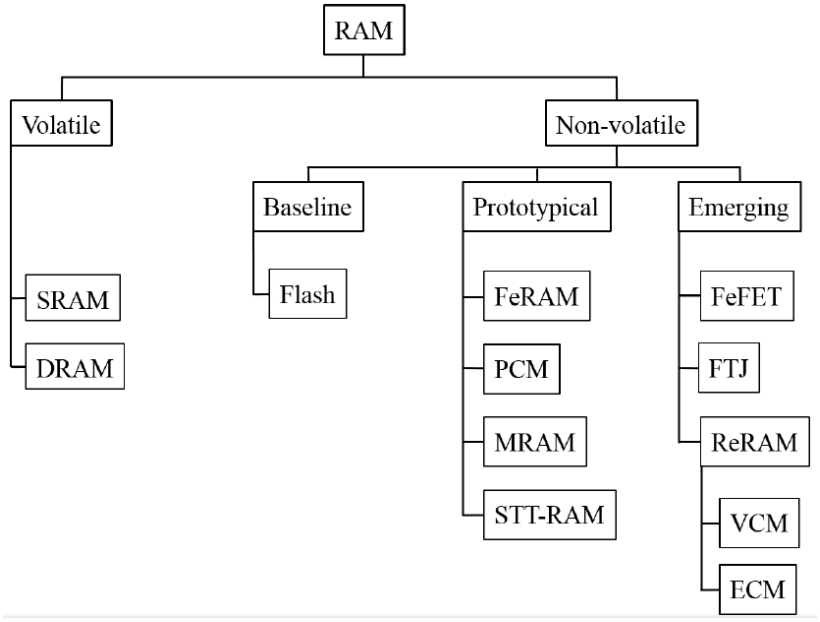

Figure 2.1: A classification of the many RAM technologies that just displays the most important types. According to the technological level of development, non-volatile RAM is categorized into baseline, prototype, and emergent memory. Adapted from [23].

As far as non-volatile technology is concerned, Flash memory (floating gate memory) is currently the most commonplace technology [24]. It is Flash technology that is one of the bases for the exponential growth of portable applications, such as digital cameras, cell phones, and other personal devices. However, Flash technology is currently confronted with the limits encountered in the miniaturization of transistors. Other technologies include FeRAM, which was first industrialized production of FeRAM was done in 2011 by Texas Instruments, MRAM in 2004 by Infineon, Freescale and TSMC, and PCRAM in 2008 by Intel and STMicroelectronics. However, in comparison to Flash technology, their applications are still confined to limited markets.

Over the past two decades, another technology has attracted the attention of microelectronics technologists: resistive memories, otherwise known as Resistive RAM - ReRAM). Very recently, the first integrated chip based on resistive RAM to provide combined operation of memory and logic was demonstrated [25]. Furthermore, because to its extraordinary broad scalability, structural simplicity, faster switching speeds (10 ns), low power consumption, longer retention life (>10 years), and nondestructive readout, ReRAM technology is deemed more attractive than the other options [26]. The ReRAM technology has been reported to be one of the most promising memories in terms of integration and performance and will be discussed next in details.

2.1.1 Static and Dynamic Random Access Memory (SRAM/DRAM)

The word “static” indicates that the memory retains its content as long as it is powered. The SRAM cell uses six transistors and no capacitor; thus, the size of each cell is important, and this limits the use of SRAM for memories with low density of integration. While the access to the data is faster and the consumption is lower, it is expensive.

Unlike the SRAM, the DRAM must be constantly refreshed in order to maintain the data, hence the term "dynamic". A DRAM memory cell consists of a capacitor and a transistor. The DRAMs

can be used in applications requiring a high density of integration also costs less in contrast to SRAM.

2.1.2 Flash memory

A Flash memory is based on the structure of a MOS (Metal Oxide Semiconductor) transistor with a floating gate [27].

One of the main limitations is the reduction of the tunnel oxide thickness. The thinning of the tunnel oxide is indeed limited by charge loss mechanisms, either intrinsic (charge evacuation by direct tunneling) or extrinsic (charge evacuation through defects, or stress induced leakage current) [24]. Other drawbacks of Flash memories are low endurance, low write/erase speed, and high operating voltage. To overcome these challenges, interest in alternative technologies has grown considerably in recent years. Even several research efforts are currently underway to explore new concepts to replace Flash technology.

2.1.3 Ferroelectric RAM (FeRAM)

These memories are based on ferroelectric effect. Ferroelectrics are polar materials with low crystal symmetry producing two equilibrium states of spontaneous polarization in the absence of an external electric field [28]. They are characterized by polarization vectors that can be re-oriented in two opposite directions by the application of an external electric field. The two orientations of the polarization allow a binary coding of “1” and “0”, representing the “ON” and “OFF” states, respectively. The polarization states in a ferroelectric crystal are due to displacements of positive metal ions and negative oxygen ions in opposite directions [29]. These two states are thermodynamically stable and can be switched from one state to the other by application of an external field (called a coercive field), which causes a characteristic hysteresis

cycle. Hence, no applied field (or voltage) is required to maintain the two polarized states, which is the basis of non-volatile memory [30].

2.1.4 Magnetoresistive memories (MRAM)

The MRAM cell comprises of two magnetic layers separated by a thin layer of a dielectric material acting as a barrier. These memories are designed to have two different magnetic states, resulting in a high or low resistance state, which can be maintained without energy input [31]. These memories employ a structure exploiting tunneling magnetoresistance. When the magnetization of the magnetic layers is parallel, the resistance is low (i.e. binary state "1") while when the magnetization is antiparallel, the resistance is high (i.e. binary state "0") [32].

2.1.5 Phase Change RAM (PCRAM)

PCRAM memory is based on the passage of a material between the amorphous state and the crystalline state, caused by the heating of the material. This phase change leads to a change in electrical resistance (information storage). The advantages of this approach are that the change in resistance is more than an order of magnitude, and its simple structure (phase change material sandwiched between two electrodes) reduces the number of steps in the fabrication process. Generally, the amorphous phase has the high electrical resistance than the crystalline phase. The operation is therefore based on a fast and reversible transition between the highly resistive amorphous phase and the low resistive crystalline phase [33]. The operating mode is based on two steps: the first one is to apply a threshold voltage which consists of heating the material by Joule effect beyond its crystallization temperature, and thus obtaining the crystalline phase; the second step is the amorphization step, where the material is heated beyond its melting temperature, liquefied, and then frozen in its amorphous phase by fast lowering of the voltage. For this reason, it can be seen that the current level for the second stage is higher. The general drawbacks of this technique are the inevitable generation of Joule’s losses for the operation and

the limited choice of materials to provide the desired effect. PCRAM is a typical representative of a unipolar resistive RAM.

2.2 Bipolar Resistive Random Access Memory (ReRAM)

Bipolar Resistive Random Access Memory (ReRAM) works by reversibly changing the resistance across a dielectric material via bias reversal contrary to PCRAM that operates with different durations and amplitudes of the same bias. A ReRAM cell has a very simple structure. It is a metal-insulator-metal (MIM) device as shown in figure 2.2.

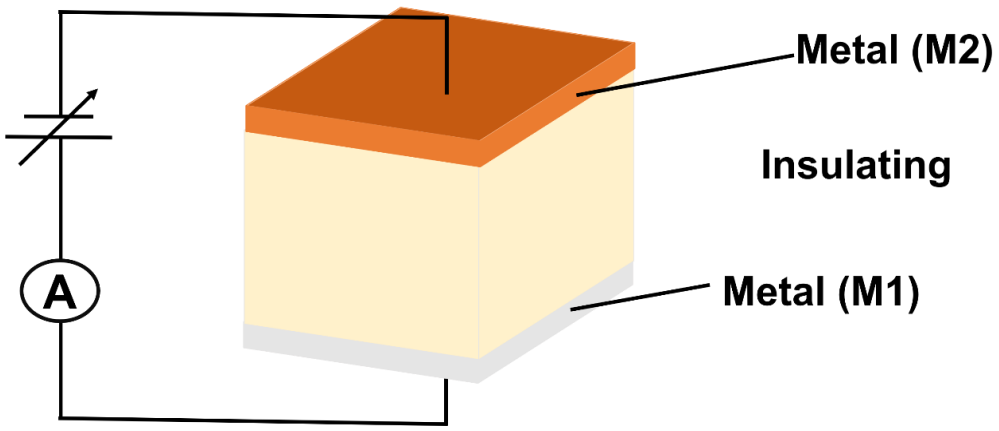

Figure 2.2: Diagram of a ReRAM memory cell that resembles a capacitor and has two metal electrodes sandwiched by an insulating or semiconducting oxide. The metals do not need to be different; an intrinsic asymmetry may as well be introduced during electroforming or the first writing cycle.

A ReRAM is based on the fact that some MIM structures show a change in resistance (or resistive transition) following the application of a voltage. Initially, the MIM structure has a high resistance ((HRS), or OFF state). When the potential difference across the structure is increased, at a certain voltage value the device goes into the conductive state, otherwise known as the low resistance state ((LRS) or ON state). Under appropriate conditions, the device may further be switched back

to an insulating state. Switching between the OFF and ON states is done by applying a certain voltage of opposite polarity ("bipolar" mode, the most general, figure 2.3b). In some cases, it is possible to switch back to an insulating state by applying a voltage of the same polarity ("unipolar" mode, figure 2.3a) [34]. Based on the underlying switching mechanism, the repeatability of the process may be anywhere between a single event (write once, read multiple "WORM" devices) and 10^{12} [35] [36]. We thus have a structure with two levels of resistance (insulator/conductor), with the possibility of switching from one to the other by simply applying a voltage: these devices can be used to create rewritable non-volatile memories. This makes ReRAM devices very attractive and much less limited in terms of miniaturization [37].

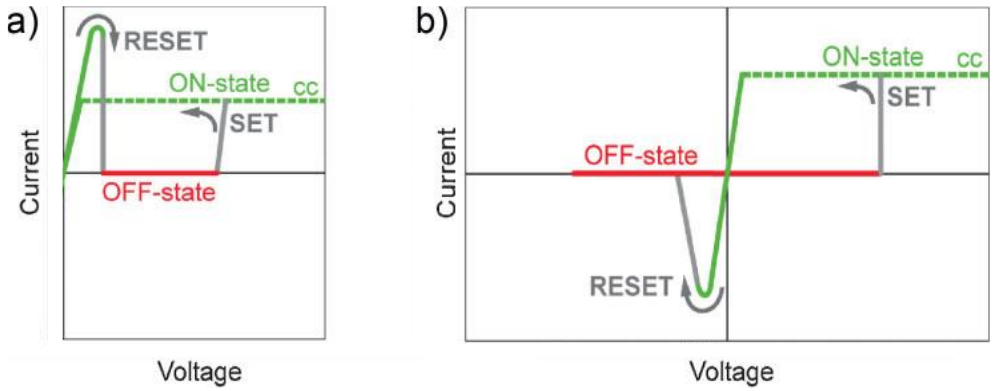

Figure 2.3: The two fundamental operating systems for memory cells that use resistive switching. I-V curves recorded for a voltage signal with a triangular shape [4].

Switching from one state to the other is achieved by applying two voltages known as V_{SET} and V_{RESET}. V_{SET} is applied in order to switch the system from the OFF to the ON state, and the ON to OFF state transition is triggered by the applying V_{RESET}. It is worth mentioning that some the ReRAM memories require a procedure called "electroforming". This is applied to a blank memory, and it is identical to the SET procedure except that it requires a voltage higher than the SET voltage or over an extended time. Finally, during the SET process, marked by the transition from the OFF state to the ON state, the current flowing through the memory cell is limited by the

external electrical circuit (the electrometer or a resistor in the case of laboratory measurements, or a transistor in the case of integrated cells. This current limit is called "current compliance ". This current compliance plays a very important role because at the time of SET switching, the current rises sharply, so that the memory cell can be irreversibly damaged if nothing is done to limit thermal runaway (irreversible breakdown of the dielectric). Therefore, the role of the current compliance is to avoid the permanent breakdown of the dielectric. It should be noted that, for the case of unipolar devices, the current compliance used for SET switching must be deactivated during RESET because the RESET current is generally higher than the compliance current (the reset may not take place if a limit current is maintained). The compliance current is therefore unnecessary for RESET switching in unipolar devices.

2.3 Resistive switching mechanism in ReRAM

Bipolar resistive switching is subdivided into two major domains depending on whether the insulator that is sandwiched between the metal electrodes plays an active or a passive role in the operation of the memory cell.

The large variety of MIM structures that exhibit resistive switching suggests, that the underlying mechanisms, that may occur simultaneously and compete with each other, have some close commonalities.

For the case of active materials, several theoretical models have been proposed to explain the resistance switching. The most relevant ones are presented in the following sections. These models can be classified into two groups, depending on whether the resistance transition involves a volume or an interface effect. A volume effect means that the origin of the resistance transition lies in the volume of our cell. On the other hand, an interface effect means that the switching phenomenon is controlled by the metal/oxide interface. For the case of passive materials, where the insulator is essentially only a porous medium allowing for the formation of

a metal filament connecting both electrodes, there is broad consensus about the mechanism [38].

2.3.1 Migration of metal cations from the anode (CBRAM type resistive memories)

Cations that are formed through electrochemical oxidation at an electrochemically active anode (e.g. silver, gold, copper) will migrate towards the negatively charged cathode to be reduced and deposited there. The subsequent growth of a filament will then give rise to a conductive path across the insulating layer. This phenomenon leads to the resistive memories of CBRAM type (Conducting Bridge ReRAM).

The MIM system is composed of (i) an anode which is an "electrochemically active" metal, i.e. capable of supplying cations which will be injected into the oxide (so-called "active" electrode); (ii) the insulating layer is a passive, porous spacer between both electrodes allowing for the drift and/or diffusion of metal ions (iii) a cathode constituted of an "inert" metal, i.e. not supplying any cations to the oxide (electrode called "inert"). The SET process starts at the anode/oxide interface, where the anode atoms are oxidized and injected into the oxide. Under the action of the field, these metal cations will migrate towards the cathode. Once the metal cations reach the cathode (inert electrode), they will capture electrons and thus reduce (electro-crystallization) to form one conductive bridge. Once the bridge is formed, forming a short-circuit between the electrodes, the voltage breaks down stopping the growth of other dendrites that might have been growing in parallel – a “winner takes it all” scenario. During the growth of the metal filament, the potential of the filament is that of the cathode, which prevents its oxidation (dissolution). Thus, during SET, the filament grows from the inert electrode (cathode) to the active electrode (anode). When the filament reaches the anode, the device switches to the ON state [39]. As shown in figure 2.4. After reversing the polarity of the applied voltage, the inert electrode becomes anode, and the active electrode becomes cathode. By increasing the potential difference beyond a certain value (V_{RESET}), the metal filament will be oxidized again and dissolved

in the insulator. Due to the conical shape of the filament, the resistance of the metal cone is higher at the top.

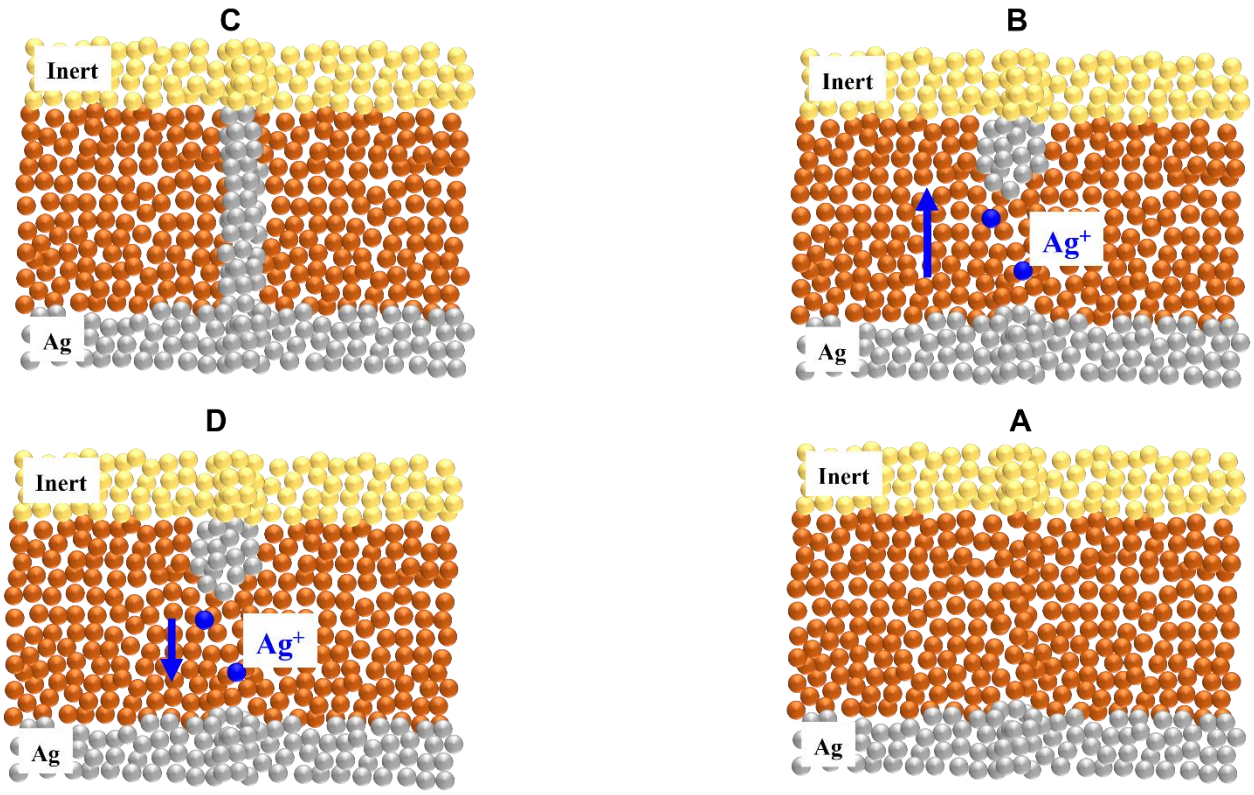

Figure 2.4: Bipolar switching of the ECM memory: (A) filament development in the high resistance OFF state, (B) filament growth, (C) the low resistance ON state, (D) filament dissolution in the reversed voltage state. Adapted from [40].

It is thus at this point that the potential gradient (the electric field) is the highest. Therefore, it is at the top of the cone that the dissolution is initiated. During the RESET phase, the filament will retract from the active electrode (new cathode) towards the inert electrode (new anode). Thus, the atoms previously involved in the SET process will be recovered by the active electrode (new cathode) and the OFF state is restored [4]. In general, once the filament is generated during an initial electroforming step, the subsequent operation is much faster as it only relates to the opening and closing of the gap between the filament and the cathode. Typical changes in

resistance between the insulating OFF state and the metallic ON state are in the range of four to six orders of magnitude.

2.3.2 Valency change mechanisms

2.3.2.1 Interface effect (modification of the Schottky barrier via oxygen vacancies)

In several models, resistance switching has been mentioned as being related to an interface effect [41], providing variable in-series resistances. In a metal/semiconductor junction, when the two materials are in contact, electrons are exchanged between the two materials until the Fermi levels of the semiconductor and the metal align. For an n-type semiconductor, a band curvature appears on the surface due to a deficit of electrons (which have transited from the semiconductor to the metal).

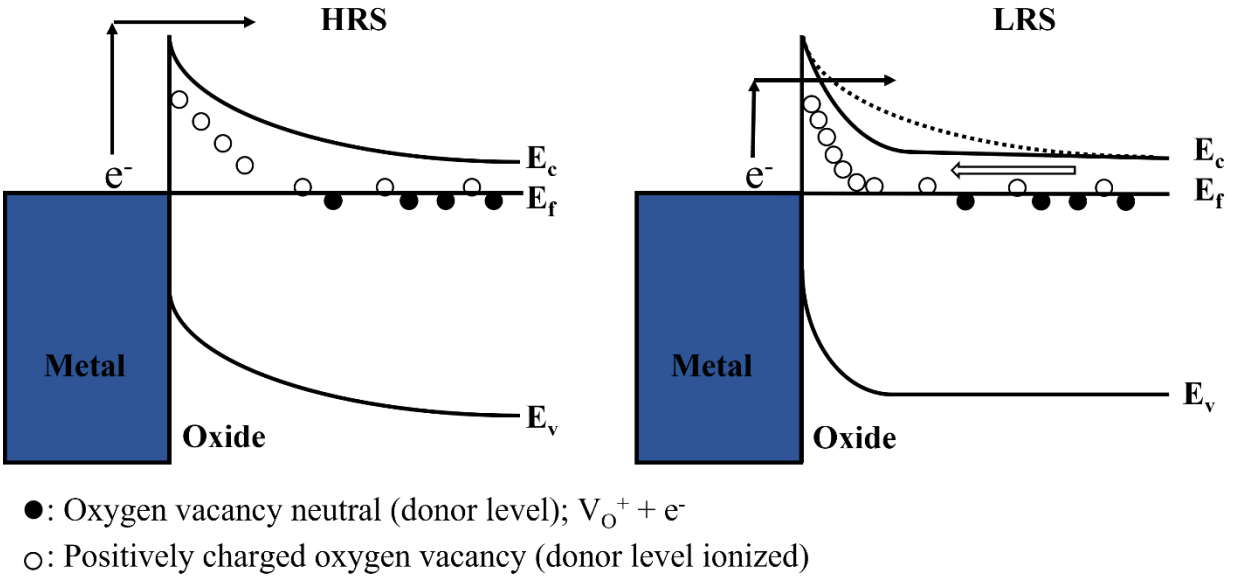

Figure 2.5: Illustration of the Schottky effect-induced resistance switching phenomena. The positively charged vacancies move toward the metal (cathode) when a negative voltage is given to it. The Schottky barrier narrows due to an increase in the density of ionized donor levels at the interface (promoted tunnel effect).

The electrons coming from the metal must overcome an energy barrier corresponding to the gap between the Fermi level of the metal and the top of the conduction band of the semiconductor [41]. This energy difference is called Schottky barrier. In this model, the resistance switching phenomenon is considered to be related to the modification of the Schottky barrier (modification of the barrier width and/or height) due to the movement of oxygen vacancies [42]. Oxygen vacancies are common defects, encountered in most oxides (studied for ReRAMs, such as WO_3 for example).

The oxygen vacancies act as donor dopants. These oxygen vacancies lead to modifications of the Schottky barrier, with a consequent variation of the interface current. Indeed, the oxygen vacancies (positively charged) will migrate towards the cathode [43]. As the grain boundaries are fast diffusion paths (even at reduced temperatures), the vacancies will follow the grain boundaries, or even dislocation planes, to accumulate at the cathode. If the applied voltage is reversed, the vacancies turn back to the cathode (former anode). The barrier width increases, preventing the passage of electrons by tunneling effect (OFF state). In this model, the switching takes place only at the interfaces.

2.3.2.2 Oxygen vacancy filaments

In many oxides, especially transition metal oxides, oxygen vacancies are easily formed or annihilated through exchange of oxygen with the ambient atmosphere. For charge neutrality reasons, oxygen vacancies carry a nominal charge of -2 given that the oxygen that was previously occupying the site was in a 2- valence state but left the sample as molecular and therefore charge neutral oxygen. This charge of -2 implies that oxygen vacancies are responsive to external electric field and will drift under external bias. ZnO- and WO_3 structures are two representatives of structures that exhibit significant semi-conduction for common concentrations of oxygen vacancies, while being insulators in their stoichiometric structure. In this case, resistance switching is often attributed to the creation of aggregated oxygen vacancies in the oxide. Under

bias, oxygen vacancies are generated in the oxide (redox reactions at the anode or breaking of metal-oxygen bonds under the effect of energetic electrons) [4]. At the same time, oxygen ions (O^{2-}) are created. The oxygen ions migrate to the anode, while the oxygen vacancies (positively charged, V_O^{z+}) migrate to the cathode. Upon reaching the anode, the oxygen ions lose their excess electrons, which can lead to the release of oxygen gas or oxidation of the anode. At the cathode, electrons will be injected on the oxygen vacancies (ionized donor levels, V_O^{z+}) and will be able to reach the anode by jumping mechanisms between vacancies. A current therefore flows in the device (ON state). Thus, the conduction paths in the oxide are considered to be composed of oxygen vacancies [44] (figure 2.6) or, similarly, to be composed of sub-stoichiometric oxygen phases with a higher conductivity than the stoichiometric phase. It is therefore the generation of oxygen vacancies that plays a primary role in the behavior of these metal oxides. This class of ReRAMs, based on the presence of oxygen vacancies (and oxygen ions), defines the resistive memories of the OxRAM type (Oxygen based ReRAM). Typical changes of resistance in an OxRAM cell between the initial insulating OFF state and the semiconducting ON state are in the range of one to two orders of magnitude, therefore somewhat inferior to the changes between an insulating OFF and a metallic ON state in CBRAM. However, like in CBRAM, the filament is a parallel resistance to the insulating layer, while the interface effect discussed above represents an in-series resistance. With a stronger ON/OFF ratio in CBRAM as compared to OxRAM, there are two different lines of argument to consider: for one, the best choice of circuitry 1T1R versus crossbar array for the integration of each technology, which will not be addressed here and for the other, the opportunity to produce OxRAM through a sinter-free process, which drastically reduces the production time. This will be discussed in more detail in the following chapters.

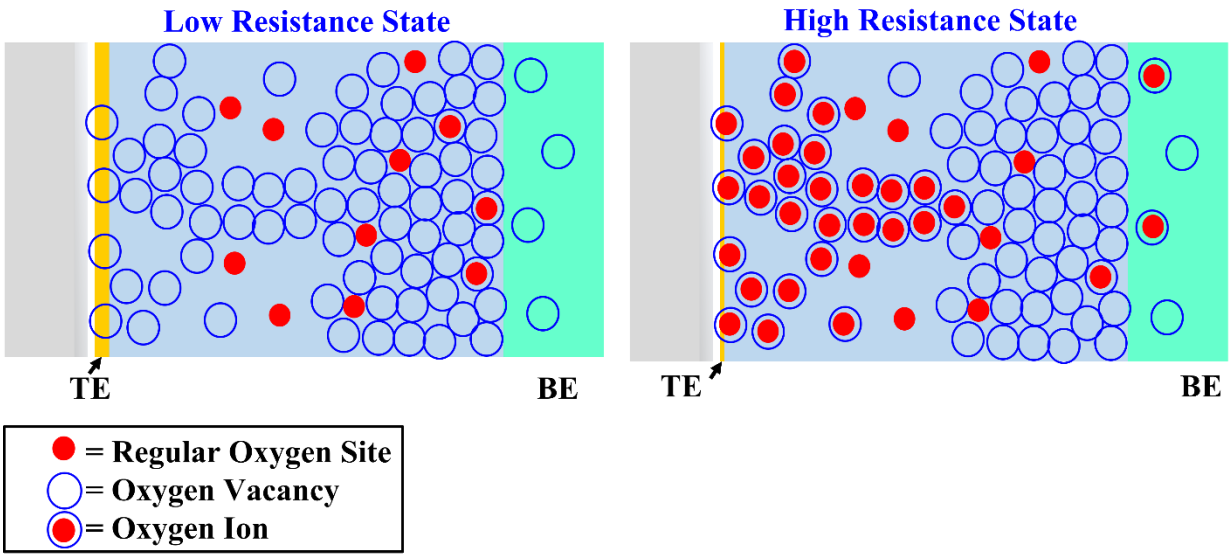

Figure 2.6: The formation (destruction) of the conductive filament made up of oxygen vacancies. BE and TE denote bottom- and top electrodes respectively.

As explained above, any case of filamentary switching regardless of whether it is through the formation and migration of metal ions or oxygen vacancies comprises two fundamentally different periods: first, the formation of the filament, referred to as electroforming and secondly, the operation of the device, where resistance switching is obtained either through a partial dissolution of the filament (without any need to fully destroy it) or the change of the barrier height for charge carriers to access the filament. Whether or not an explicit electroforming step is required depends on the combination of a) film thickness and b) number and mobility of the species creating the filament. In many cases, especially for very thin films as in our case and investigations with quasi-static current-voltage sweeps, the electroforming occurs at time scales that are faster than the I-V measurements, so that it appears to not be explicitly necessary. This may however change if the device is only to be operated under pulsed conditions, where individual pulses may be insufficient to generate a filament.

2.4 Electrode and Solid Electrolyte Materials

The basic characteristics of the materials utilized in the conductor-insulator-conductor sandwich stack of memory cells are covered in this part. In chapter 4, the numerous diverse material compositions with a cell consisting of three single layers are discussed. The materials are detailed in depth in this section. The conducting polymer poly(3,4- ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) serves as bottom and top electrode while nanoparticles of WO_3 or ZnO in porous layer act as the insulating matrix and the functional material for resistive switching.[1]

The printed top and bottom electrodes are made of organic polymer PEDOT:PSS, which is a conductive, transparent, and ductile material. As a result, it has become one of organic electronics key workhorses, with applications in organic light emitting diodes, solar cells, and field-effect transistors [45][46][47]. PEDOT:PSS is a mixture of cationic PEDOT that has been oxidatively doped and is electrostatically bound to a PSS anion [48]. A dried film's morphology is anisotropic, with lentil-shaped features that are tens of nanometers in size. Individual grains have a PEDOT-rich core and a PSS-rich shell, which are bound together by hydrogen bonds formed by PSS's sulfonate groups. The electrical conductivity is caused by charge carriers hopping and is strongly dependent on the morphology of the PEDOT:PSS [49]. Organic solvents interact with PEDOT chains, causing them to alter structure and uncurl. Because of the increased mobility, this can greatly boost conductivity [50]. The top and bottom electrodes are made of Heraeus CleviosTM P Jet N V2 PEDOT:PSS ink, which is a common inkjet ink for organic electronics. It has a dynamic viscosity of 22.5 mPa·s, a density of 1.00 g/cm^3 and a surface tension of 24.8 mN/m.

[1] PEDOT:PSS is known to undergo electroreduction, which bears the natural question whether it contributes to the resistive switching. Experiments with PEDOT:PSS alone have shown that there is no detectable contribution of PEDOT:PSS to the resistive switching in our films in the voltage range of interest.

The WO_3 nanoparticle loose structure provides a large number of interface states and voids between individual nanoparticles. The Avantama P-10 WO_3 nanoparticle ink is made up of a 2.5 wt % dispersion of WO_3 nanoparticles of 12-16 nm size in isopropanol with a dynamic viscosity of 2.5 mPa·s, a density of 0.80 g/cm^3, and a surface tension of 20.2 mN/m. Tungsten trioxide WO_3, a binary transition metal oxide (TMO), has recently received a lot of interest for its potential use in ReRAM devices[51]. WO_3 is an n-type, wide-bandgap semiconductor with an electronic bandgap (E_g) ranging from 2.6 to 3.2 eV depending on crystallinity [52], which may be tuned to meet specific needs by adjusting nanoparticle size, the E_g decreases with size due to the quantum confinement effect [53]. It is also an important electrochromic material since it is transparent throughout the majority of the visible spectrum [54]. The presence of reducing gases (N_2), external electrical stimuli, and heat can all affect its optical transmittance[55]. In the Ɛ_WO_3 form, it might also be used as a photocatalyst [56] and thermoelectric material [57] [58]. Many investigations on WO_3 based devices have demonstrated great optical transparency [59], good retention and endurance [60], electroforming-free operation[61], and low power consumption [62].

Zinc oxide has the benefit of being optically transparent, low cost, and non-toxic under the process conditions. The insulating ZnO nanoparticles ink (Sigma-Aldrich H-SZ01034), consists of a dispersion of 2.5 wt% of ZnO nanoparticles of 8-16 nm size in isopropanol with a dynamic viscosity of 10.5 mPa·s, a density of 0.80 g /cm^3, and a surface tension of 29 mN/m. Wide bandgap semiconductors, such as zinc oxide, are widely employed in transparent conducting applications, especially solar applications [63]. Additionally, it has been utilized effectively in valence change ReRAMs[64] and electrochemical metallization [65] as an oxide layer [66]. High ON/OFF ratios have been reported for the ZnO-based conductive bridge RAMs produced by sputtering, ALD, PLD, and sol-gel due to the nature of the mechanism [67], even though there were reasonable doubts from the beginning about whether the effect was associated to ZnO or the presence of a possible electrochemically active electrode material to provide CBRAM operation.

2.5 Bending Theory

The key characteristic of flexible electronics is its resilience under mechanical deformation. This refers to both the mechanical integrity, as well as the electrical performance under repeated mechanical stresses. Out of the different types of performance characterization under stress, bending resilience is arguably amongst the most important characteristics when it comes to flexible electronics.

In the following section, we present the fundamentals of the bending process as it applies to thin structures, such as printed thin films.

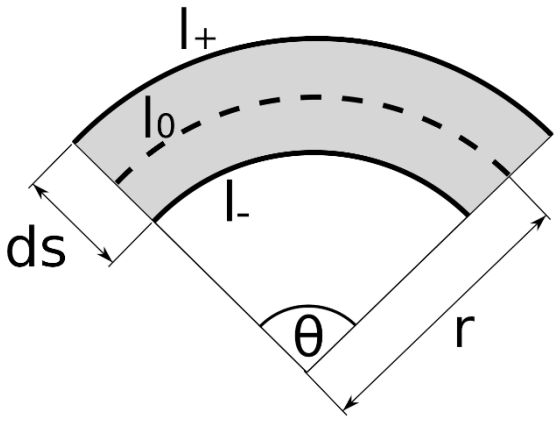

Figure 2.7: Schematic bending of the substrate. When the substrate is bent over a specific bending radius r, its middle, neutral axis remains at the initial length l_0. The outer surface is stretched to l_+ due to tensile bending, the inner surface is shortened to l_- due to compressive bending.

The bending radius r is the distance at which normal vectors on the film intersect. When a substrate of thickness d_s is bent to radius r, the side towards the intersection point is compressed, while the other side is stretched. For thin films and a linear elastic material without plastic deformation, the sides experience an equal and opposite strain ±ε, while the middle,

neutral layer of the substrate is not subjected to strain, thus its initial length remains constant, forming an arc of length $l_0 = r\theta$.

The outer surface is stretched to $\mathrm{l}_{+} = \left(\mathrm{r} + \frac{\mathrm{ds}}{2}\right)\theta$, while the inner surface is compressed to $\mathrm{l}_{-} = \left(\mathrm{r} - \frac{\mathrm{ds}}{2}\right)\theta$.

A schematic of the bent substrate can be seen in figure 2.8. The strain ε acting on deposited structures on the substrate can therefore be positive for tensile and negative for compressive bending:

$$\varepsilon(r) = \frac{l - l_0}{l_0} = \frac{l}{l_0} - 1 = \frac{ds}{2r} \tag{2.1}$$

From this equation, one can see that the mechanical deformation on the surface can be reduced by reducing film the thickness d_s. This formula neglects the contribution of printed structures on the film, which is an acceptable approximation in our case: Our printed structures are well below 1 micron thick, while our substrates have a thickness of 125 µm. In order to keep the printed structure in the neutral bending zone for future applications, a lamination step would provide an equal thickness of the substrate material above the printed structure.

Th geometrical change of a printed conductor structure also causes a change in its electrical resistance. This is caused by the chance of geometry of the conductor, and, depending on the material, an additional piezoresistive contribution. The relative change in resistance ΔR/R is linked to the strain ε by a geometrical factor k by the linear relationship

$$\frac{\Delta \mathrm{R}}{R} = k\varepsilon \tag{2.2}$$

The geometrical factor k considers both the material, as well as the geometry of the resistive structure [68]. We shall see that such piezoresistive contributions from either the filament or the electrodes are negligible.

CHAPTER 3

3 FABRICATION AND CHARACTERIZATION METHODS

3.1 Fabrication

This chapter gives an overview of the most important practical techniques, just as the fundamentals chapter covered the theoretical foundations needed for a better understanding of the results.

Inkjet printing is introduced, and then the layout of the memory cells is explained. Atomic force microscopy and electron microscopy are described as well as the methods of electrical characterization. This work describes the mechanical test setup used to determine the cells' flexibility using an in-house design, rotate-to-bend, that is built on the basis of in-house analysis techniques.

3.1.1 Inkjet printing

The advantages of additive techniques like inkjet printing over traditional device fabrication techniques that include lithography, additive and subtractive steps (etching or lift-off) are simplicity, speed, low cost, and versatility of the equipment. The deposition of small volumes of liquid, in the range of picolitres and micrometer positional accuracy provides sufficient precision for feature sizes around the resolution of the naked eye, ideally suited for displays. Drop-casting provides ease of individual droplet deposition with control over the distance between these drops and while being slower for the coverage of large areas than e.g. screen printing, it allows for an immediate patterning of surface features. Printing on flexible foils, which is equally

possible, does enable various applications in the field of flexible electronics, which is different from semiconductor technology, which is limited to rigid wafer substrates.

For drop-cast ink-jet printing, ink is driven from a reservoir through a micron-size aperture (nozzle) via a piezoelectric actuator. The piezoelectric material deforms when a tunable voltage pulse, also known as a waveform, is applied to it, and an ink droplet is pushed out of the nozzle (see figure 3.1).

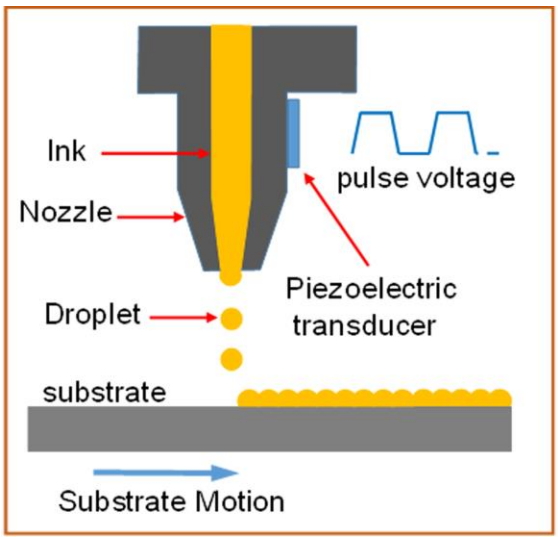

Figure 3.1: Schematic of the inkjet printing process: A piezoelectric actuator is placed close to the ink channel and the nozzle [69]**.**

The voltage pulse may be adjusted to fit a wide range of ink viscosities and surface tensions. In Appendix A, you will find all of the different waveforms for the different inks. A solution or dispersion of functional material in a liquid carrier, the solvent, makes up an inkjet ink. Metal nanoparticles, conducting and non-conducting polymers, insulators, and photochemically active compounds are all possible ingredients in inks [70].

In order to be printed, the ink must meet certain conditions regarding its fluid qualities. The inverse of the Ohnesorge number, the Z number, is a dimensionless measure used to assess an ink's suitability for inkjet printing [71] [72]:

$$Z = \frac{\sqrt{D\sigma\rho}}{\eta} \tag{3.1}$$

where D is the nozzle diameter, ρ is the density of the ink, σ is its surface tension and η its dynamic viscosity.

The range of 1< Z < 10 has been empirically proven to be suitable for drop-on-demand inkjet printing. For Z< 1, the ink's high viscosity often prevents the pressure pulse from dissipating. Satellite droplets accompany the primary droplet when Z > 10 and have an impact on print quality [73]. For values even further out of this range, the drops will either be unable to even form or the ink will leak from the nozzle.

Ink	*Viscosity (mPa.s)*	*Density ($g.cm^{-3}$)*	*Surface tension ($mN.m^{-1}$)*	*Z - number for D = 21µm*
PEDOT:PSS	22.5	1	224.8	1
WO_3	2.5	0.8	20.2	7.4
ZnO	10.5	0.8	29	2.1

Table 3.1: Z numbers for the various inks, density ρ, surface tension σ, and dynamic viscosity η

The Z numbers are based on D = 21 µm, which is the nozzle diameter of the Dimatix DMP2832 printer's DMC-11610 cartridge. Once a sequence of damped oscillations is triggered, the substrate-droplet contact stretches and comes to rest after the droplet strikes the substrate [72]. The ultimate radius, or spread of the ink droplet, is determined by the substrate's surface energy and the ink-substrate interaction, all described within the theory of wettability. Prior to printing, it can be adjusted for certain inks by washing the substrate with polar or non-polar solvents or exposing it to an oxygen plasma. For example, oxygen plasma treatment improves the hydrophilic characteristics of a substrate. As a result, a non-polar ink would spread less on an oxygen plasma-treated substrate, but a polar ink would spread more. A pattern of droplets is printed on a substrate to design a specified shape, which overlap and form the structure. Drop spacing, or the space between the drops on the substrate, is a critical aspect in printing quality and must be modified according to ink characteristics and substrate interaction. If the drop spacing is excessively large, the droplets on the substrate are less likely to overlap, resulting in gaps in the structure. If the drop spacing is too low, too much material will be deposited, causing the structure to bulge [74]. As a result, the drop spacing must be tuned for every particular ink and substrate combination.

The so-called coffee stain effect, which characterizes the tendency of dissolved material to deposit near the structure's periphery, is another major influence on the printed structure's characteristic.

The ring form of a dried coffee droplet inspired its name. At the fringe of the structure, where the contact line (meniscus) between the ink and the substrate is pinned, the evaporation rate of the solvent is larger as soon as ink droplet wets the substrate. As a result, material flows from the center to the fringe, resulting in more deposited material at the border and a larger structural feature size at the fringe. An ink with a low solvent concentration and reasonably large viscosity is best for limiting the coffee stain effect. Furthermore, increasing the evaporation rate of the entire printed structure by heating the substrate during printing minimizes the coffee stain

impact [75]. The impact can also be reduced by mixing two solvents with differing boiling temperatures [76].

3.1.2 Sintering

After printing and evaporating the solvent, a separate sintering step may be necessary for those that do not exhibit the desired properties through simple ink transfer to the surface. This includes metal nanoparticles if they are deposited with the aim to form a conductive trace. Just a few inks are completely functional without sintering, notably those based on conductive polymers, metal nanoparticle inks however need to be molten to coalesce and to form a coherent conductive layer. Other ink, including spin-on glasses may require a sintering step for form a 3D matrix with desired mechanical and optical properties. Sintering describes the controlled connection of previously only agglomerated particles mediated through external energy input. This energy is generally transferred into heat (e.g. from initial photo-sintering or microwave sintering) or directly introduced via heating.

For the case of metal nanoparticles, the requirement for annealing stems from intended and unintended coating of the nanoparticles. To stop the ink from coagulating, metal nanoparticles are often coated with a polymeric stabilizing layer. This polymeric layer represents an electric insulation between the various nanoparticles after printing [77]. Thus, for the ink to become conductive, the polymeric layer has to be removed by thermal (also combined with chemical) treatment, which also fuses the nanoparticles together to create a network of conductive pathways. Because of the large surface to volume ratio of the particles, it is important to note that the melting temperature of metal nanoparticles is significantly lower than that of bulk material. This phenomenon known as melting point depression [78]. As a result, a printed

metallic structure can be fused together at reduced temperatures close to 100 degree C, and thus attain resistivity that approaches that of bulk material [79]. Figure 3.2 shows the results of sintering a line of printed silver nanoparticles.

The sintering procedure for substrates that conduct heat can be performed on a hotplate, while poor heat conduction polymer foil substrates must be heated from the top, for example in an oven. Using an oven enclosure also enables inert gas purging during the sintering process, which stops the metal layers from oxidizing at elevated temperatures. Alternate ways to generate sintering temperatures directly on the printed structure include microwave, photonic, or electrical sintering [80][81] [82]. Unintentional coating stems from oxidative surface passivation in e.g. copper and silver nanoparticles and also requires a coalescence of the particles via sintering to form a coherent conductive layer. Usually, the layer conductivity achieved through sintering comes close but never quite reaches bulk values due to remaining voids in the layer.

Sintering is a time- and energy consuming step which however remains imperative for certain material classes including the aforementioned metal nanoparticles. To avoid this step, a different class of conducting electrode material has to be taken into consideration.

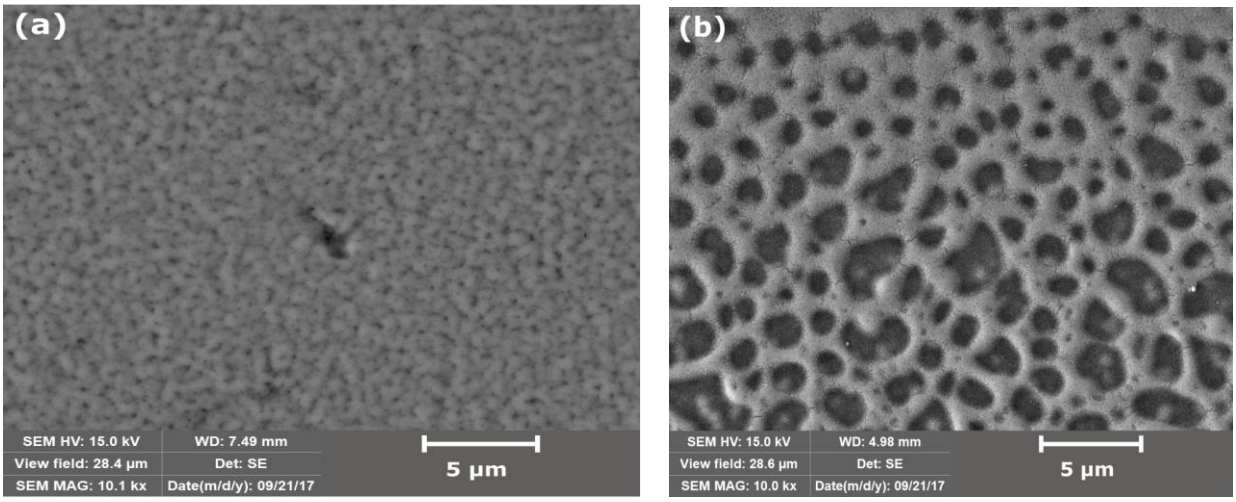

Figure 3.2: Inkjet-printed line of silver nanoparticles with 10 nm average diameter. (a) Unsintered (b) Sintered at 200°C in an oven. The sintering process leads to a densification and creates a conductive layer [40]**.**

In return, the sinter-free process allows the use of a larger variety of substrate materials, due to the absence of thermal constraints of the individual materials. Especially polymer substrates degrade during sintering, while the printed nanoparticles may oxidize at elevated temperatures. Additionally, deposited materials can start to diffuse, spread, or agglomerate during the process. Besides the direct thermal effect, the thermal expansion can introduce stress into the composite due to differences in thermal expansion, which can lead to delamination.

Besides the physical drawbacks, the sintering equipment and additional sintering step increases cost and complexity to the process. The oven and hotplate solution are affordable, but may degrade the substrate, while microwave and electric sintering generally do not provide very homogeneous heating and are relatively slow. To confine the heat more evenly to the surface,

the photonic annealing option exists, but this solution is very costly. Another requirement of annealing metals is that inert gas may be required.

3.1.3 Memory Cell Design

When arranged in a crossbar array, ReRAM cells can reach a cell size of $4F^2$. The lowest conceivable structures made possible by the manufacturing method are denoted by the minimum feature size F. In a crossbar array, the bottom electrodes' parallel lines are crossed perpendicularly by the top electrodes' parallel lines (figure 3.3a). In this configuration, the bottom and top electrodes are referred to as wordlines and bitlines, respectively. By applying voltages to the word- and bitlines of a specific cell, it may be switched and read out. Current sneak pathways across neighboring cells, on the other hand, can endanger measurements. In the LRS, neighboring cells can cause significant leakage currents (figure 3.3b).

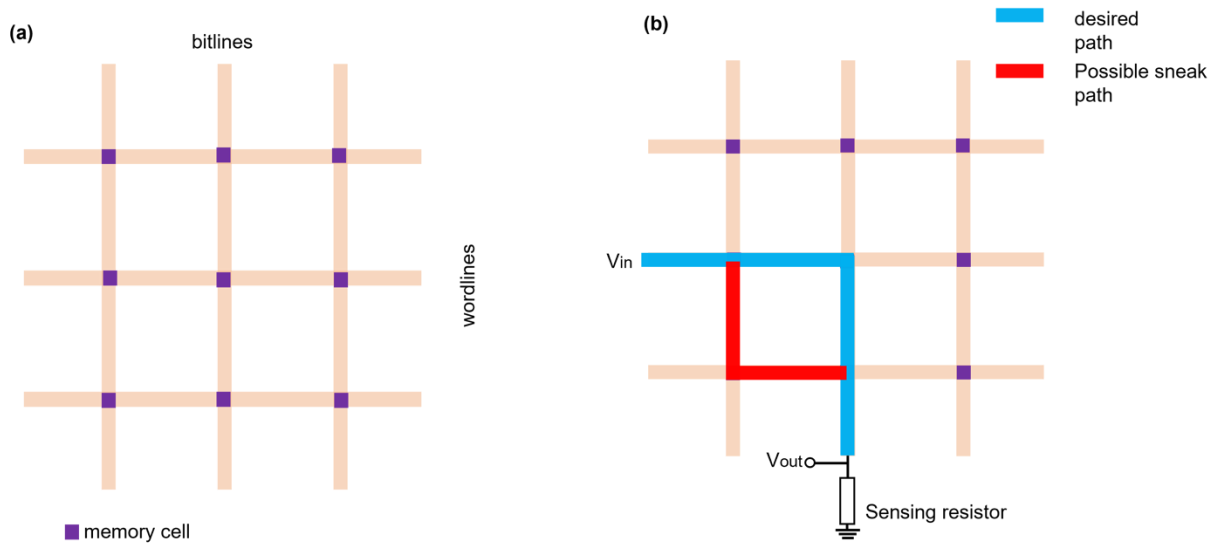

Figure 3.3: A crossbar array in which one memory cell is formed at each point where the wordline and bitline cross. (b) Sneak path issue: The target cell in the middle's intended current route is shown in blue. Neighboring cell leakage currents may "sneak" through and affect the measurement (shown in red).

There are several ways to deal with the sneak path problem. Specific read and write techniques can be employed in passive arrays. To write or read data from a cell, the wordline is charged with V_{in} and the bitline is set to ground. All other word and bitlines are charged with $V_{in}/2$ to reduce the voltage loss between the target cell and its neighbors. Another method involves placing a transistor as a selection device at each junction of the word- and bitlines, thereby suppressing any leakage currents [83]. Pn-diodes can be utilized as selection devices for unipolar devices [84]. Without the use of any extra selectors, stacking two identical memory cells on top of each other provides a complementary device that can reduce the sneak path issue [85]. This thesis, however, uses mostly structures with only one wordline and multiple bitlines to rule out any impact of sneak route currents. As a result, all measurements may be traced back to operations occurring in a single memory cell.

Three printed memory cells are shown in the diagram (figure 3.4). A wordline is formed by one PEDOT: PSS nanoparticle bottom electrode, which is coated by a layer of WO_3. The bitlines are made up of three perpendicular PEDOT: PSS top electrodes.

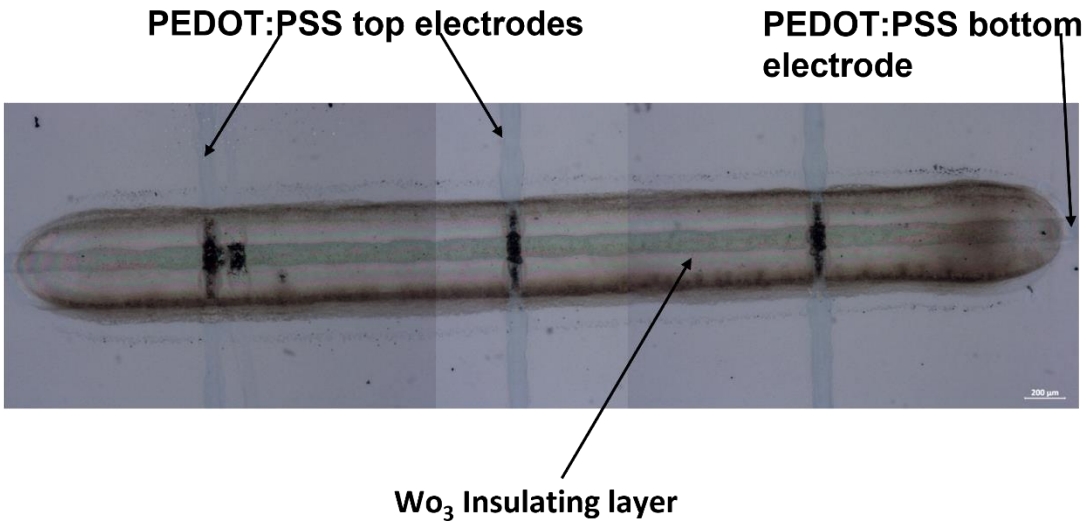

Figure 3.4: Photograph of printed memory cells with one PEDOT:PSS bottom electrode as word line and three PEDOT:PSS top electrodes as bit lines.

3.2 Analysis

3.2.1 Conductive Atomic Force Microscopy (C-AFM)

One of the most powerful and well-established methods for surface imaging at the nanoscale is atomic force microscopy (AFM). The sample surface is scanned using a sharp probe attached to a cantilever, which produces a three-dimensional picture of the topography. Piezo-electric scanners, which depend on the inverse piezoelectric effect, allow for precise placement of the probe with regard to the sample. The sample is commonly coupled to a flexure scanner for lateral raster scanning in the x-y direction. An extra linear piezo scanner paired with an optical setup detects the change in height (Δz) (see figure 3.5)

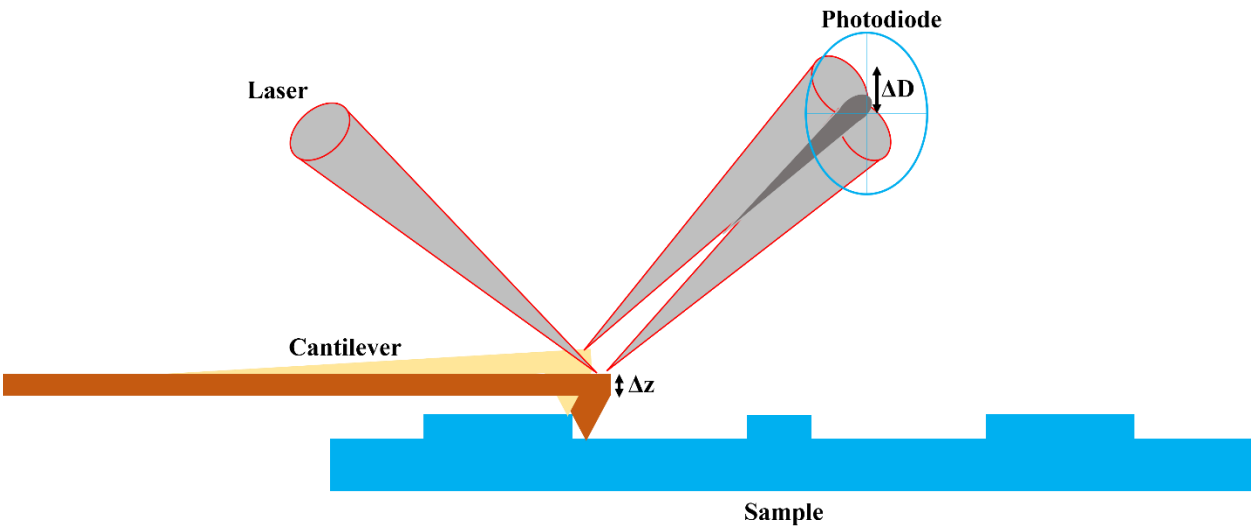

Figure 3.5: An AFM's basic operating concept. The cantilever bends due to a change in topography caused by Δz, and this causes ΔD to deflect the laser spot on the photodiode.

The cantilever bends when the tip contacts the sample surface due to attractive Van-der-Waals forces or Pauli repulsion. A laser beam is reflected off the cantilever onto a four-sector photodiode, and the change in the laser spot position as a function of ΔD shows cantilever deformation on the sample. The z-piezo scanner's feedback loop uses the deflection of the laser

light on the photodiode as a feedback signal. The tip is always in mechanical contact with the sample surface when scanning in contact mode, and the laser deflection, i.e. cantilever deformation, is kept constant. High scan rates are possible with contact mode operation, but the combined lateral and normal pressures degrade the tips and are detrimental to the image resolution. Conductive atomic force microscopy (CAFM, also known as spreading resistance microscopy) is a method that needs the probes to be coated with conductive layers like Pt, Au, or doped diamond [86]. The tip is electrically connected to a measurement circuit and acts like a mobile top electrode. The electrical characteristics of the sample can be examined simultaneously with its topography by introducing a voltage between probe and sample during scanning. It is worth noting that the coating increases tip diameter, resulting in lower lateral resolution. Furthermore, lateral stresses can cause the coating to degrade or delaminate, and high current densities at the tip's apex might cause it to melt. CAFM allows for both sample current mapping and local current-voltage measurements. In order to alter the sample locally, continuous voltage or current-voltage-sweeps can be applied to the resting tip. All AFM and CAFM measurements are carried out with an AIST-NT SmartSPM 1000 system, which has multiple current ranges for scanning and local current-voltage-sweeps of 1 nA, 100 nA, and 10 µA. For the conductivity measurements, Applied NanoStructures Inc.'s Pt/Ir-coated ANSCM-Pt probes with a tip radius of 30 nm were employed. A 1MOhm or 10 MOhm compliance resistor is in series to the sample in the circuit to limit the current and to protect the AFM current amplifier.

3.2.2 Electrical Characterization

Complete valency change memory (VCM) cells are measured using a two-point probe station, whereas two-layer structures with active bottom electrode and insulating layer may be measured electrically with the CAFM setup with the Pt-coated tip functioning as inert electrode. With micrometer manipulators, two tungsten needles (diameter 12 µm) are positioned on the contact pads of the top and bottom electrodes. For electrical characterization of VCM cells, two main modes of operation can be used: quasi static voltage sweeps and voltage pulses. Quasi-static

sweeps provide exact switching voltages, whereas voltage pulses provide information on switching speed and can lead to an approximation of the amount of charge required for the SET process and allow for an investigation of fatigue resistance. Device operation will usually occur in a pulse scheme.

A Keithley 2400 Sourcemeter, which can set a current compliance between 1 nA and 1.05 A with a voltage step time of 80 ms, is used to do quasi-static voltage sweeps. The step size of the staircase sweep is 0.01 V for all triangle voltage sweeps from 0 V to a positive voltage, returning to 0 V, followed by a negative sweep to a negative voltage and back to 0 V. It should be mentioned that the current compliance in place is meant to prevent excessive currents to irreversibly alter the devices. However since the individual I-V measurements for increasing voltages are tens of milliseconds apart with current integrations times also in the range of tens of milliseconds, the SET event may lead to a very large current across the sample during the one measurement that exceeds the set voltage. Only when the current compliance circuit detects that the threshold was exceeded, it will from then on control the maximum current. So, the exposure of the device during the unique SET event, is somewhat outside of a detailed experimental control and leads to certain fluctuations of experimental data. In comparison to the usual voltage pulse duration of a memory device in the range of nanoseconds (our experimental unit is limited to tens of microseconds), the speed of the current compliance setup is very slow, about a million times slower than the operating pulses, so the effect may be substantial.

A Keysight B2091A Precision Source/Measure Unit (SMU) was used for the quasi-static electrical measurements. It provides a voltage sweep functionality with configurable current compliance. This is necessary to prevent any hard electric breakdown, which may occur in the memory cell for large currents and leads to an irreversible transition to the ON state. The voltages are sufficient to do a separate electroforming step, if required.

3.2.3 Profilometer

The thicknesses of the printed structures are determined with a Veeco 150 profilometer, using a 12.5 µm tip radius. Given the relatively soft nature of the printed polymers, the error on the total thickness is relatively high while the reproducibility remains good.

3.2.4 X-ray diffraction measurements

A four-circle X-ray diffraction with PANalytical X'pert Pro diffractometer equipped with a Cu $K\alpha_1$source ($\lambda = 1.5406$ Å) is used to investigate the crystal structure. The diffraction pattern is recorded in the range between 30° - 80° in the Bragg-Brentano configuration (Θ-2Θ) with a 0.02° step size.

3.2.5 Transmittance measurements

Transmittance spectra are recorded using a Stellar Net BLUE-Wave (350-1150 nm) spectrometer linked to an Olympus BX41 microscope to analyze the device's optical features. The light source is a 100 W halogen lamp.

3.2.6 Mechanical Characterization

A key benefit of the inkjet printing process is that flexible substrates such as polymer films can be used. When printing electronic structures with functional inks, the resilience of the device under mechanical deformation needs to be assessed. There exist several different types of these stress tests [87].

In our experimental setup, we decided to test the performance of printed conductive lanes under various bending radii. The mechanical automation of the setup permits testing for the smallest bending radius before sudden device failure, as well as the progressive breakdown under repeated bending cycles. Various bending setups have been proposed in literature, including the push-to-flex setup that flexes the sample in an unguided way [88]. The roller-flex setup bends the sample over a cylindrical roller of fixed diameter, which has the challenge of possibly introducing additional forces [89]. The flex-e-test setup holds the sample under tension between two fixtures and drags it over a convex surface [90].

Harris et al. [87] formulated the following characteristics of an ideal bending test setup:

- Uniform strain over the entire sample
- Reproducible, well-defined bending parameters, i.e. strain and strain rates
- Minimize contact with the sample to avoid interfering with the electronic structure
- Automated in-situ measurement of relevant device parameters, e.g. electrical resistance

Only the push-to-flex setup avoids touching the sample during compressive bending. This disqualifies the other variants, as it can damage the electrical connections, as well as the printed structure. However, the push-to-flex design cannot perform consecutive sequences of tensile and compressive bending, which may occur in typical applications. For this reason, our groups designed a device that conforms to the above-mentioned requirements, including consecutive bending in both compressive and tensile mode.

Our rotate-to-bend apparatus clamps one side of the sample, while the other one can rotate around a defined axis as shown in (figure 3.6) The angle β defines the angular offset relative to the unbent position. Depending on the direction of rotation, tensile or compressive strain is generated on the printed surface [91].

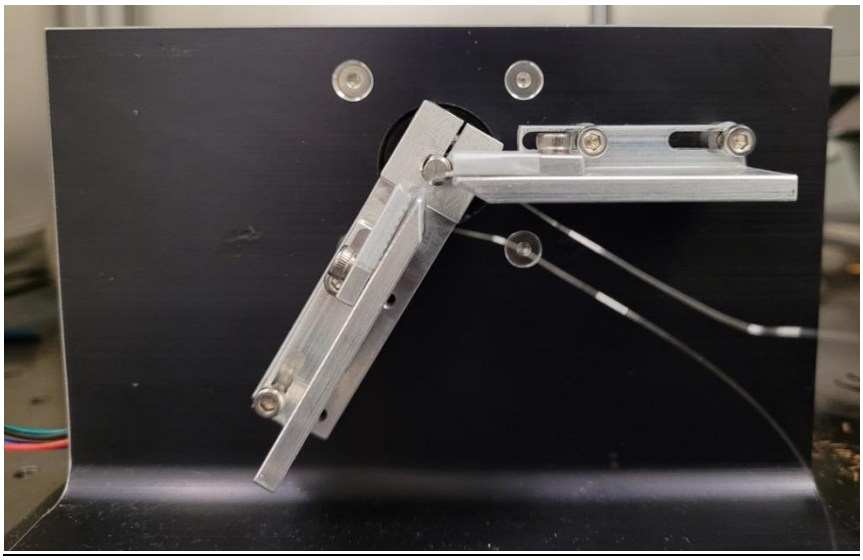

Figure 3.6: Photo of the rotate-to-bend apparatus with the fixed right clamp and the rotatable left clamp. Both clamps are movable on their guide rail to set the spacing L between them.

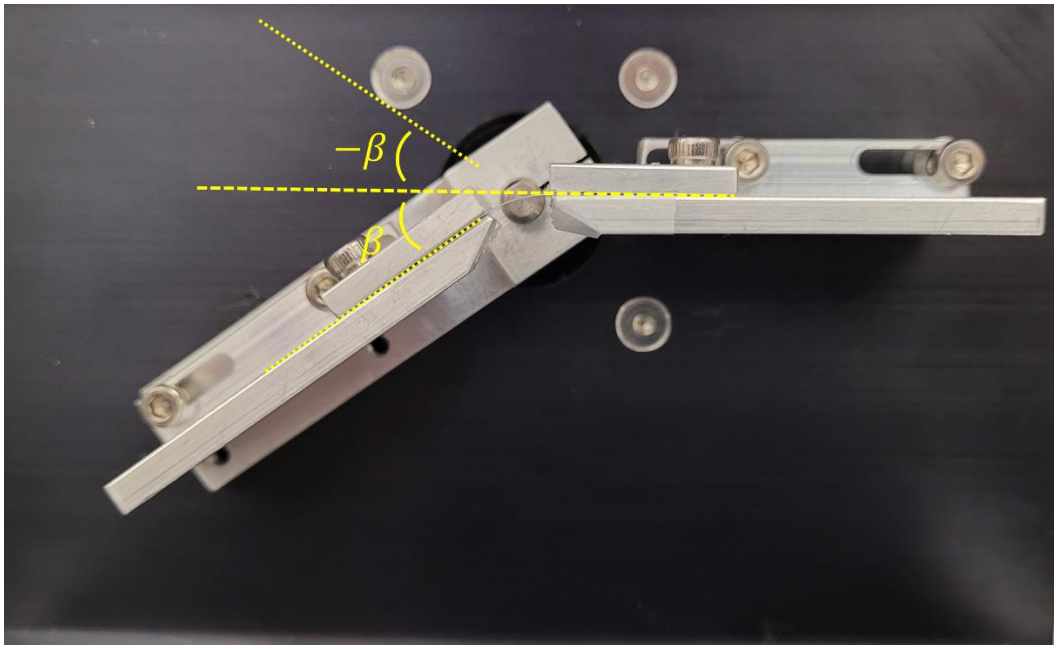

Figure 3.7: Side-view photo of the bending setup with the bending angle β in the image plane.

The bending is automated using a stepper motor (RB-SOY-03), which is controlled by an Arduino UNO R3 microcontroller that is controlled by the measurement computer via serial USB connection. For in-situ electrical measurements, flexible copper wires are attached to the foil by

silver paint to PEDOT:PSS top electrodes. In our setup, a Keithley 2400 SMU is employed to generate both writing and reading pulses for the resistive memory elements.

Since the bending radius in this setup is minimal in the center of the clamps, the printed structure must be centered precisely to exert reproducible strains. The bending radius can be expressed as a function of the angle β and the distance between the clamps L. This flexing is approximately equal to a push-to-flex setup with unclamped ends, which can be approximated by the following equation [Park et al.] [92]:

$$r(dL) = \frac{L}{2\pi\sqrt{\frac{dL}{L} - \frac{\pi^2 d_s^2}{12L^2}}} \tag{3.2}$$

In this equation, dL is the shortening of the initial sample length L in the horizontal linear stage due to the bending, and d_s is the substrate thickness. Although this formula describes an unguided bending with an unclamped substrate, it can still be applied to the setup where the substrate is tightly clamped in the grips. The bending in the rotate-to-bend setup is very similar to free bending because the clamps fixing the substrate are rotated as well and follow the rotational motion. However, while the linear stage of a push-to-flex setup is determined by dL, the determining variable for the rotate-to-bend apparatus is the angle of rotation β. Therefore, dL is substituted by β. The formula thus becomes

$$r(\beta) = \frac{L}{2\pi\sqrt{\left[1 - \sin\left(\frac{180° - |\beta|}{2}\right)\right] - \frac{\pi^2 d_s^2}{12L^2}}} \tag{3.3}$$

In principle, this formula describes only the bending radius r of the middle plane of the substrate. Thus, the exact bending radius acting on the printed memory cell is different by half of the substrate thickness. Since our substrates remain below 125 µm, this contribution can be

neglected. The formula only considers absolute values of β, so we keep track of compressive/tensile measurements separately.

CHAPTER 4

4 RESULTS AND DISCUSSION

In the following sections, we present our study of two inkjet-deposited oxide materials: ZnO and WO_3. Both oxides are studied in MIM structures, using the flexible, transparent PEDOT:PSS material to form ReRAM memory cells. The PEDOT:PSS ink is the commercially available Clevios P JET N V2.

4.1 PEDOT:PSS/WO_3/PEDOT:PSS Memory cells

This section details the manufacturing parameters and performance results of the MIM memory element. The three-layered memory cell structure consists of WO_3 sandwiched between PEDOT:PSS, using the drop-on-demand process and parameters detailed in section 3.1.1. The width and height of the deposited structure is determined by the profilometer described in section 3.2.3.

4.1.1 Fabrication process

First, the PEDOT:PSS bottom electrode is printed on flexible polyethylene naphthalate (PEN) foil. The drop spacing is 25 µm, the line width is ∼200 µm. Using a stack of 5 layers, a layer thickness of approximately 150-200 nm is obtained. Next, the WO_3 nanoparticle ink (12–16 nm) is printed with a drop spacing of 5 µm as the insulating layer. A stack of 8 layers is printed on top of the PEDOT:PSS. Finally, the top electrode is deposited with identically to the bottom electrode, perpendicular to the bottom electrode to form the cross-point structure. The drop spacing and the number of layers for PEDOT:PSS are the result of an optimization process to achieve high and reproducible conductivity for the thinnest possible film while the same optimization for the WO_3

layer was targeting sufficient thickness to avoid leakage between top- and bottom electrode through the porous nanoparticle layer. Thicker films of WO_3 had no beneficial effect on this property but caused more use of ink, longer electroforming times/energies, and less flexibility.

The temperature during the printing process is regulated, which allows controlling the ink properties and the accelerate the drying process. For the bottom electrode, 60°C is maintained, which allows the ink to merge into a homogeneous and narrow line. A lower temperature of 30°C was used for the WO_3 layer followed by 60°C for the top electrode. No post-deposition treatment such as sintering was performed.

4.1.2 X-ray diffraction measurements of WO_3 insulating layer

The WO_3 crystal structure was studied using four-circle X-ray diffraction with PANalytical X'pert Pro diffractometer equipped with a Cu $K\alpha_1$source. ($\lambda = 1.5406$ Å). The measurement was done in Bragg-Brentano configuration $(\theta - 2\theta)\ \text{scan from}\ 30°$ to 80°. The counting time was 3 s/step with a 0.02° step size. The acquired XRD pattern of the WO_3 insulating layer is shown in figure 4.1 Although the peaks are not well-defined, yet the presence of somewhat broadened peaks confirms the insulating layer is not amorphous. The pattern exhibited a much intense diffraction peak at 2θ≈27 corresponding to the (111) orientation. However, other diffraction peaks were also shown to be asymmetric and are indexed to the reference pattern with JCPSD #: 18-1418. While there are no peaks attributed to a secondary phase, the as-purchased WO_3 ink is shown to compose of nanoparticles with a wurtzite structure. The substantial peak broadening is attributed to finite grain sizes (Debye-Scherrer equation) while the peak asymmetry of the (111) peak is a possible indication of surface relaxation effects in WO_3 nanostructures.

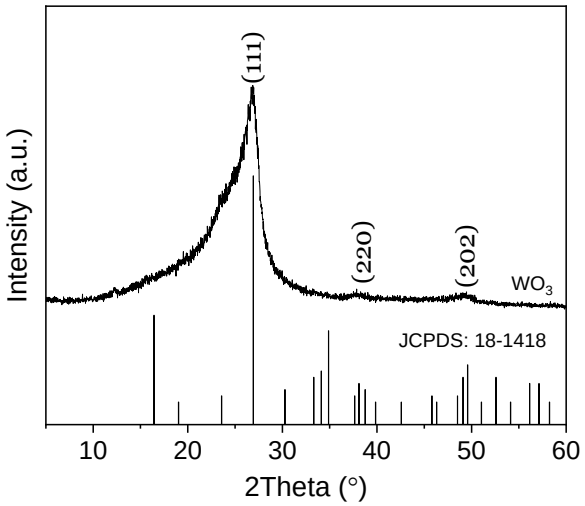

Figure 4.1: X-ray diffraction pattern of WO_3 layer deposited at room temperature

4.1.3 AFM surface topography

An AIST-NT Smart SPM atomic force microscopy (AFM) system was used to perform surface topography imaging and spreading resistance measurements, also known as conductive AFM. The maps are acquired in conductive AFM (C-AFM) mode by applying an electrical bias potential through a conductive ∼30 nm radius Pt−Ir coated Si tip acting as a mobile top electrode and placed in contact with the film surface.

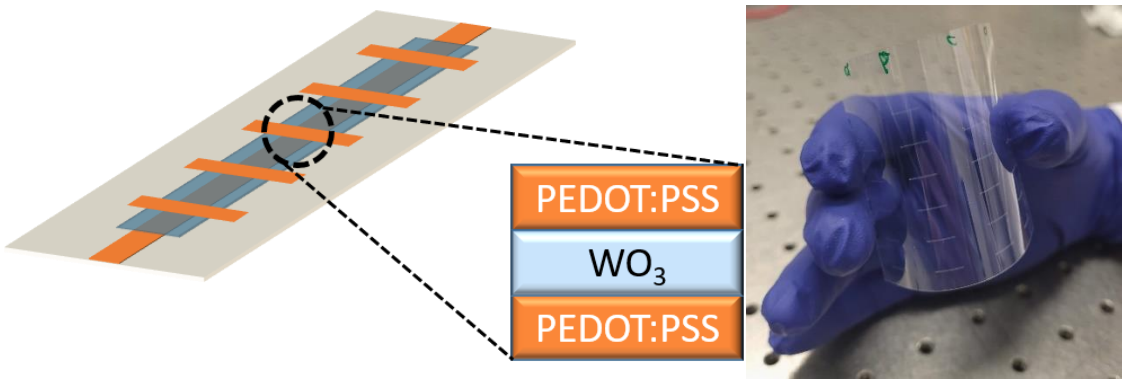

Figure 4.2: Schematic representation of the flexible crossbar array of devices (left). The inset shows a magnified single device cross section consisting of a thin WO_3 insulating layer and two PEDOT:PSS electrode layers. On the right, is the printed device indicating the transparency and flexibility of the device [93].

4.1.4 Conductive-AFM: Spreading resistance

Figures 4.3a and 4.3b show the current map and surface topography of the pristine state of the WO_3 layer. Figure 4.3c depicts the current map for the samples after -9 V bias was applied to a square section in the central portion with an area 500nm x 500nm. A subsequent scan with a read voltage of -0.1V unambiguously reveals a region with higher conductivity compared to the pristine region outside. The corresponding surface morphology, seen in figure 4.3d, shows morphological features consisting of nano-sized grains. The surface morphology shows a granular microstructure which is similar in the biased and unbiased regions and does not provide indications of topography changes upon resistive switching. The color contrast in the current map clearly indicates a localized effect that was attributed to the formation and migration of oxygen vacancies as they cluster. Initially, the oxygen vacancies are uniformly distributed across the surface and the bulk of the sample. As the applied voltage increases, the oxygen vacancies begin to cluster and form conductive channels across the thickness of the film. Consequently, we observe an increase of current flow across the sample as the sample transitions from HRS state to LRS state. However, throughout all these voltage sweeps, the surface morphology does not change.

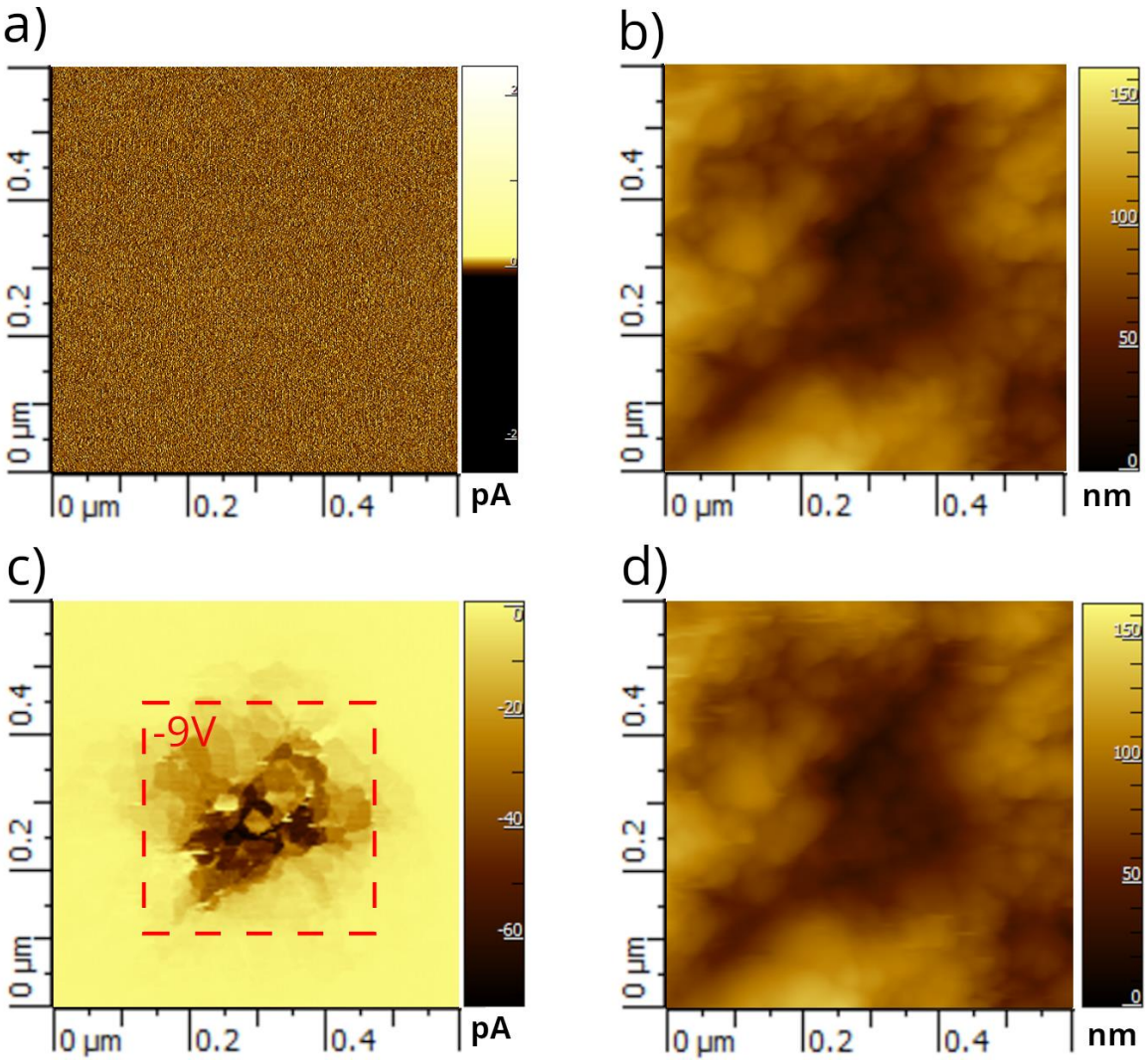

Figure 4.3: Surface and current maps of the PEDOT: PSS/WO_3/PEDOT: PSS memory cell. a) Current map of the pristine state, b) Surface topography of the pristine state, c) Current map obtained at a bias voltage of -0.1V and d) Surface morphology after filament creation. For the case of WO_3, it was not possible to achieve a reversible switching of the filament under the conditions described above. This is attributed to the formation of a permanent filament (hard breakdown) as the conductive AFM operates without current compliance circuit rather than with an in-series resistance.

4.1.5 Current-voltage characteristics upon resistive switching

The printed cell structures are shown in figure 4.2. A Keysight B2091A Precision Source/Measure Unit (SMU) was used for the quasi-static electrical measurements with a voltage step size of 10 mV and voltage sweeps between 4.5 V and -4.5 V. A current compliance was set between 100 nA and 100 mA. This is to prevent any hard electric breakdown, which may occur in the memory cell for excessively large currents. No separate electroforming procedure was needed to activate the memory cells.

Figure 4.4 shows a typical I-V switching curve measurement. The switching is characterized with two distinct switching behaviors viz: i) analogue switching from HRS (1) to LRS (2) state in the positive cycle; and ii) analogue reset switching from LRS (2) to HRS (3) in the negative cycle.

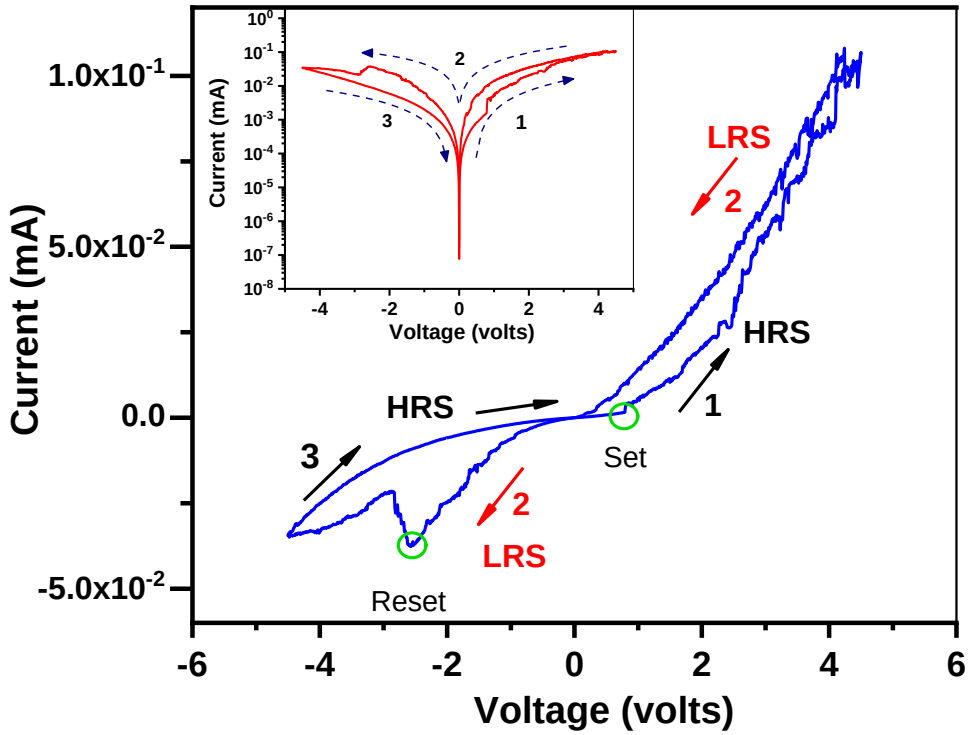

Figure 4.4: Typical I–V switching curve recorded on a PEDOT:PSS/WO_3/PEDOT:PSS cell. The inset shows the absolute value of the current on a semi-logarithmic scale.

The quasi-static sweep consisted of individual electrical measurements along a sawtooth voltage profile with time steps of 0.05 sec and voltage of 0.02 V. The cells are observed to transform from the high resistance OFF-state to the low resistance ON-state at a voltage of approximately +0.8 V and return back to OFF for the opposite polarity at approximately 2.5 V. In order to protect the memory cells from current surge, an external compliance current of 1 mA was set. With the features such as low write and erase voltages, and small operating currents, the memory devices have the capability of operating at low power consumption.

Moreover, electroforming is not necessarily required to trigger the first switching cycle upon the quasi-static conditions. It appears as if the formation of oxygen vacancies as the first step of electro-forming occurs at a lower voltage than the observed switching voltage and that the exact switching voltage observed under quasi-static conditions was a function of the voltage sweep rate.

4.1.6 Interpretation of the eletrical behavoir

The overall nature of the switching curve is of analogue type, which indicates the homogenous oxygen ion movement in the whole device. The movement of oxygen vacancies and trapping/detrapping of electrons determine the bipolar switching activity in oxide materials. By various means such as hopping between adjacent sites under the influence of the electric field, moving along a dislocation, grain boundaries, surfaces, interfaces etc., oxygen vacancies can easily move around the sample. A number of processes like the Poole-Frenkel emission, space charge limited conduction (SCLC), and trap assisted tunneling (TAT) have been established as channels through which electrons can be trapped/detrapped. The mechanism of the charge conduction in the dielectric oxide is broadly categorized into two classes and this depends on the properties of the dielectric (bulk limited) and the interface between the dielectric and the electrodes (interface/electrode limited) [25]. For films thicker than 10 nm, the Schottky emission will be the most likely interface limited mechanism. This is known to arise from a difference in

Fermi levels between the metal electrode and the insulator/dielectric. A potential barrier is created as a consequence of the energy difference the metal and insulator. The charges therefore must overcome this barrier under adequate thermal activation in order to enter the insulator. Accordingly, the current density across a Schottky barrier is given by equation [17]:

$$J_{Schottky} = AT^2 exp\left[\frac{-q\phi_B}{k_B T} + \frac{\sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{k_B T}\right] \quad (4.1)$$

where *A* is the Richardson constant, ϕ_B is the height of the Schottky barrier, *E* is the electric field across the dielectric, k_B is the Boltzmann constant, *T* is the temperature in kelvin, ε_r is the relative permittivity of the dielectric and ε_0 is the absolute permittivity of the vacuum. For a Schottky emission, the plot of ln (J/T^2) vs $E^{1/2}$ should be linear.

Furthermore, when the medium hosts the traps (in this case oxygen vacancies), there will be a transition of the charge carriers into the conduction band once the material is thermally activated. Such a phenomenon is referred to as the Poole-Frenkel (PF) emission. This kind of emission occurs due to reduction in potential energy of trapped electrons under the influence of external electric field, which in turn increases the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric material. Similar to equation (4.1) above, the current density due to a PF emission under the influence of electric field E is given as [95]:

$$J_{PF} = q\mu E N_c exp\left[\frac{-q\phi_T}{k_B T} + \frac{\sqrt{qE/\pi\varepsilon_r\varepsilon_0}}{k_B T}\right] \quad (4.2)$$

where, μ is the mobility of the charge carriers in the dielectric medium, ε_r is dielectric constant, ε_0 is the absolute permittivity of vacuum, N_c is electron density of states in the conduction band,

$q\phi_T$ is the trap energy. The PF emission is usually dominant at both high E and T. For a preliminary inspection, the plot of Ln(J/E) vs $E^{1/2}$ should be linear.

Poor conductivity is a typical characteristic of dielectrics, as they are generally wide bandgap semiconductors. This culminates to the formation of a space charge region between the electrode and metal interface. This interfacial space charge impedes the flow of further charge into the dielectric, a phenomenon referred to as the space charge limited conduction (SCLC). It is known to depend on the conductivity of the dielectric layer. As such the current density arising from the SCLC is expressed as [17][95]

$$J_{SCLC} = \frac{9\mu\varepsilon_r\varepsilon_0\theta V^2}{8d^3} \tag{4.3}$$

where the symbols have the same meaning as discussed before. The term θ expresses the ratio of the free carrier density to total carrier (free and trapped) density. For SCLC mechanism, the plot of J vs V^2 is linear. Additionally, a typical plot of log J vs log V is bounded by the three regimes, namely, Ohm's law ($J_{\text{Ohm}} \propto V$), traps-filled limit (TFL) ($J_{\text{TFL}} \propto V^2$), and Child's law ($J_{\text{Child}} \propto V^2$). Figure 4.4 shows the current-voltage characteristics plotted for different conduction mechanisms for positive and negative voltage cycling. In principle, the plot of log J vs log V aides in the identification of the different regimes of SCLC mechanism. As observed from the plot, the Ohm's law region (slope ~1) is clearly demarcated from the Child's law region (slope ~ 2). In the event that Schottky emission controls the current flow in the dielectric, a plot of $\ln(J/T^2)$ vs $E^{1/2}$ will give a better description of the conduction mechanism. The same is true for the Poole-Frenkel ($\log(J/E)$ vs $E^{1/2}$) mechanism. The fitting for SCLC model is shown in figure 4.5a and 4.5b. The linear fits to plot of J vs V^2 are shown in figure 4.5b, and log J vs log V plot figure 4.5a. Figure 4.5a clearly reveals two regions, Ohmic (V<0.80 volts) and Child's law (V> 0.80 volts). Figure 4.5c and figure 4.5d show current-voltage characteristics for Schottky and Poole-Frenkel mechanisms, respectively. In both the positive and negative cycles, linear regions in current-voltage

characteristics are present. However, the positive cycle is slightly distinct from the negative with respect to the presence of a step in *y* ordinate corresponding to 0.88 in *x* ordinate. This *x* ordinate corresponds to V=0.76V in figure 4.4, earlier identified as the forming voltage. To distinguish between the various conduction mechanisms, it is necessary to identify the correct values of dielectric constant ε_r deduced from the fitting and compare with the expected value. For instance, reported values of ε_r for WO_3 films is in the range, ~3-6 [96][97]. Table 4.1 shows the various derived parameters. The SCLC model yields ε_r~ 9 and 4 for the positive and negative cycles, respectively. The linear fitting with Schottky mechanism yields a value of ~ 5 for the dielectric constant in the positive cycle and ~ 6 in the negative cycle [98].

Parameters	SCLC cycle		Schottky cycle		Poole Frenkel cycle	
SI units	+ve	-ve	+ ve	-ve	+ ve	- ve
θ ratio of free carriers /total carriers	10^{-3}	10^{-3}	-	-	-	-
ε_r dielectric permittivity	9	4	5	6	-	-
μ(cm^2/Vs) carrier mobility	12	12	-	-	12	12

Table 4.1: Fitting parameters for various conduction mechanisms in PEDOT:PSS/WO_3/PEDOT:PSS cells

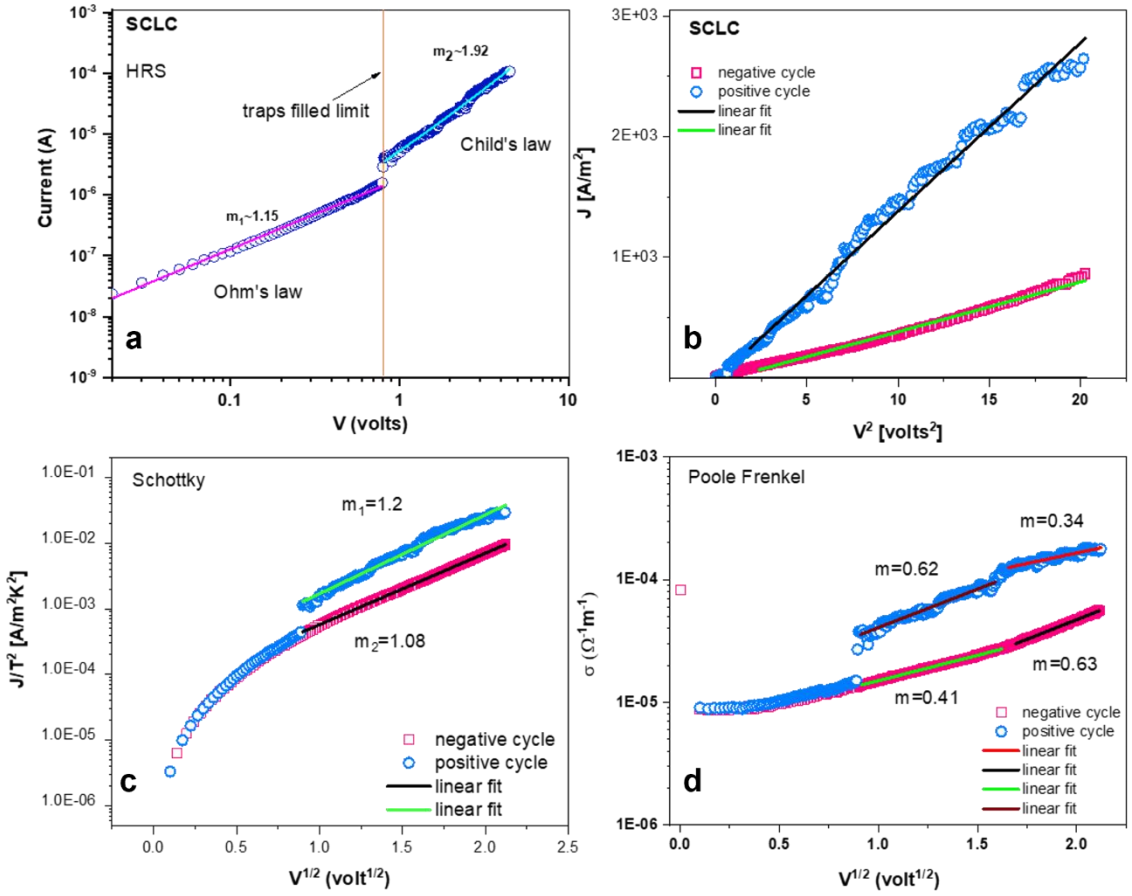

Figure 4.5: Fitting of the I-V characteristics to the different conduction models (a and b) SCLC (c) Schottky and (d) Poole-Frenkel.

4.1.7 Endurance and Retention

The ability to endure and retain information are the major parameters to be considered in order to assess the performance of a memory device. While retention is the measure of a device to retain the information stored over a period of time, endurance refers to sustainable performance of device over bipolar switching cycles without fatigue or significant loss of functional characteristics (the respective resistance values for the ON and OFF state and their ratio). To evaluate the endurance of the devices, the resistances of the LRS (ON) and HRS (OFF) on a single crossbar at a read voltage of 0.5 V over 6000 cycles using a pulsed switching sequence with

write/erase pulses with an amplitude of 3.5V/-3.5V and a width of 0.1 s are recorded. For the retention, a single pulse of 3.5V/-3.5V with a duration of 0.5 s to set/reset the device was applied. In reading the ON/OFF states over time, we use a pulse of 0.5V and a width of 0.1 s applied every 1 minute. The retention and endurance data for the devices are shown in figure 4.6. The HRS and LRS states were distinguishable up to 80000 s, when the low resistance state cannot be attained anymore. For one of the samples from the same batch, the stability and discreteness of the ON/OFF states remain up to 6000 cycles.

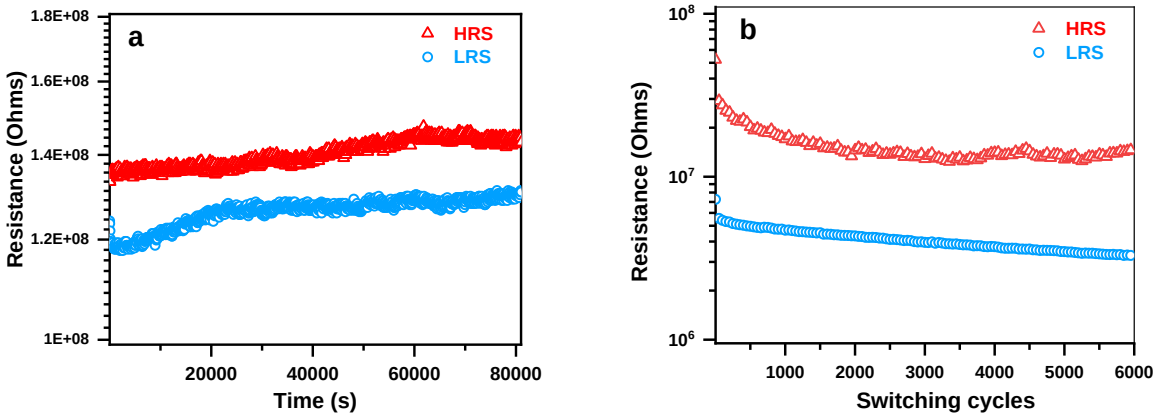

Figure 4.6: Retention and resistive switching response of the PEDOT:PSS/WO_3/PEDOT:PSS memory cell (a) Retention behavior of PEDOT:PSS/WO_3/PEDOT:PSS memory cell (b) Pulse induced resistive switching response over repetitive bipolar switching cycles

4.1.8 Discussion

The presence of charged species causes a polarity-dependent current conduction, which reacts to applied electric field. In oxides, this is due to the presence of oxygen vacancies, which are positively charged or due to the electronic transport from trapping and de-trapping of electrons [26][99]. Oxygen vacancies are point defects, which are in thermal equilibrium and their presence reduces the Gibbs free energy of the system. Using Kröger-Vink notation, the creation of oxygen vacancies in metal oxides can be expressed as:

$$O_o \rightleftharpoons \frac{1}{2} O_2 \uparrow + V_O^{\bullet\bullet} + 2e' \quad (4.4)$$

From the equation above, oxygen vacancies can be regarded as positively charged species. Therefore, the condition of electroneutrality requires that the two electrons be generated for each oxygen vacancy, $V_O^{\bullet\bullet}$ created. When an external electric field is applied, the oxygen vacancies move towards the cathode whereas electrons move towards the anode. The various ways in which oxygen vacancies can induce resistive switching are [36][51]: (1) Oxygen vacancies tend to cluster and form conducting filaments under the influence of an electric field, (2) modulation of Schottky barrier at electrode-oxide interface due to motion of oxygen vacancies under an external bias. The electric field modifies the distribution and density of the oxygen vacancies which in turn affects the height and width of the Schottky barrier leading to a change in the electrical resistance [100], (3) oxygen vacancies can also form trap sites for electrons inside the Schottky barrier region. In this case, the Schottky barrier can be modulated by the neutralization of the oxygen vacancies due to the trapping of electrons. The movement of oxygen vacancies can occur along the grain boundaries [101], disordered surfaces at the interface [102][103], forming a conducting pathway across the cell. On the other hand, electronic conduction takes place through Poole-Frenkel emission or trap-assisted tunneling of the electrons across the cell. The built-up of the charge at the interface between the oxide and the metal electrodes could lead to space-charge limited conduction (SCLC). This bulk limited phenomenon arises due to the build-up of space charge (immobile) due to injection of charges from metal electrodes into the dielectric at a rate faster than that could be dissipated [104]. As a result, the charge built-up opposes any further charge injection and limits the current across the device. While the majority of studies show a linear or Ohmic relationship between the voltage and current in LRS state, the HRS state can have diverse conduction characteristics, such as Poole–Frenkel emission, Schottky emission, the space charge limited current (SCLC), trap assisted tunneling (TAT) etc. Trap-assisted tunneling usually occurs in very thin films (<50 Å) due to the

presence of gate oxide traps and has been found to be the dominant conduction mechanism responsible for stress induced leakage currents (SILC) in stressed transistors [105]. When a negative voltage is applied to the tip of AFM, the oxygen vacancies are attracted to the surface of the sample near the tip. They cluster to form conducting filaments whose number and size increases with applied negative bias to the sample. As a result, we observe a more conducting region in the current map (figure 4.3c). The current conduction is dominated by the ionic conduction by oxygen vacancies. Under the influence of the positive tip voltage, the, $V_O^{\bullet\bullet}$ at the surface are repelled and they agglomerate at the grain boundaries. They do not participate in current flow and the conduction is mostly due to the movement of electrons resulting in a weak current due to low density of states in a dielectric. However, the oxygen vacancies at the grain boundaries act as traps for the electrons. This creates a space charge region and further lowering of the current due to the electron flow and requires fairly high voltage to de-trap the electrons (depending on trap depth) for a significant flow of charge across the device. To understand the mechanism of charge transport, the I-V characteristics of the device were analyzed as shown in figure 4.4 switching characteristic, which is polarity-dependent and features characteristic of oxygen vacancy switching is observed. While both SCLC and Schottky mechanism provided good fits to the J-V characteristics with reasonable values of various physical parameters including ε_r, it appears that SCLC is the dominant mechanism at low voltage (<2 V) whereas Schottky emission starts to dominate at higher voltages.

4.1.9 Bending-induced fatigue for the PEDOT:PSS/WO_3/PEDOT:PSS cell

A PEDOT:PSS/WO_3/PEDOTT:PSS cell was subjected to 700 bending cycles with a bending radius of 3.1 mm. The electrical response of the sample due to mechanical stress sample was studied using the set-up described in section 3.2.6 (figure 3.6). A priori, filamentary switching is expected to be insensitive to macroscopic bending radii as the diameter of the filament is so small compared to the attainable bending radii (that are anyways larger than the substrate thickness within elastic theory) that the properties of the filament are barely affected. In our case, the

conducting AFM experiments indicate an upper limit of the filament diameter in the range of a micron. This value is strongly overestimating the actual size of the filament under operation with a top electrode as the electroforming conditions – as previously discussed – without current compliance are not conceived to obtain thin filaments. And even so, with a filament diameter in the range of a micron, this is still about hundred times smaller than the substrate thickness and about thousand times smaller than the bending radii discussed. A bending radius of 3.1 millimeter already comes relatively close to folding the substrate even though folding would strictly speaking no longer be reversible. The HRS and LRS obtained at a readout voltage of 0.5 V are shown in figure 4.6. In order to discriminate changes in the electrical resistance of the memory cell (WO_3) against changes in the electrical resistance of the electrode (PEDOT: PSS), an electrode line was subjected to the same bending cycle process. The resistance of the single electrode line is obtained by fitting a linear function to the Ohmic I-V plot. The electrode resistance variation ($\Delta R/R$) as a function of the number of bending cycles is plotted on the right axis of the graph in figure 4.7. When the number of cycles increases, the resistance of the single electrode line increases. As it is a stepwise process, the resistance increases gradually, starting from 31.8 kΩ until it reaches a state where the conduction along the PEDOT: PSS electrode breaks down. This can be understood assuming that the substrate starts to form cracks or is splintering along the bending axes, thus deforming and leading the electrode towards failure as reported by Zardetto et al [106].

The ON/OFF ratio for the cell under study remained relatively constant for the first 100 cycles. The degradation of the ON/OFF ratio obtained at 700 cycles was associated with the degradation of the substrate, inducing the breakdown of the PDOT:PPS electrode. Due to this substrate effect on the electrodes, the mechanical resistance of the memory can no longer be tested beyond 700 cycles. The replacement of this substrate with a more mechanically resistant substrate such as 25 µm, or 50 µm [91] would be necessary to perform mechanical strength experiments for a higher number of cycles. With this being said, 700 cycles provide more than enough margin for applications in smart tags and disposable electronics (metro tickets etc.)

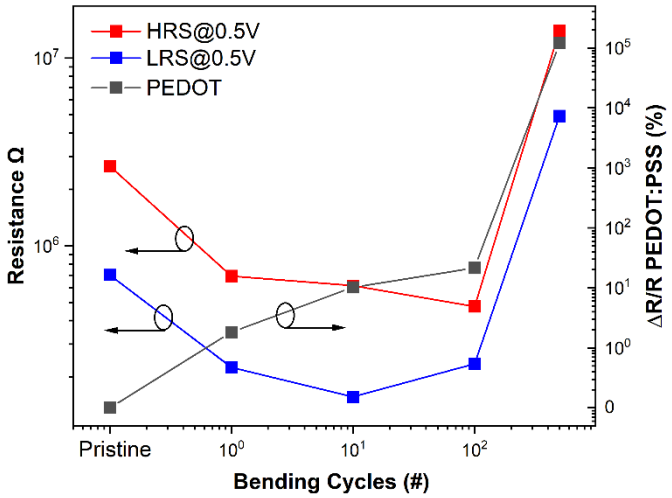

Figure 4.7: Evaluation of the flexible memory's bending abilities. The squares show the resistance values for HRS and LRS measured at 0.5V (in various colors). A PEDOT:PSS electrode's relative resistance change is represented by the triangles. The matching Y-axis is denoted by the arrows on the illustration.

Clearly, figure 4.7 shows that mechanical failure upon consecutive bending is not about the resistive switching material and the filament therein. It is rather associated to the loss of conduction in the electrodes that fail due to the formation of cracks. More crack-resistant electrodes (e.g. carbon nanotube-based) may provide an alternative to PEDOT:PSS while preserving a similar performance for transparency.

4.1.10 Transmittance measurements of WO_3 insulating layer

To study the optical properties of the device, transmittance spectra were acquired on a Stellarnet BLUE-Wave 350-1150 nm spectrometer coupled to an Olympus BX41 microscope. A 100 W halogen lamp was used as the light source. The transmittance of a complete memory cell deposited on a polyethylene naphthalate substrate is depicted in figure 4.8. The insert in the figure corresponds to an optical image of one of the devices, where the label in the background

can be visible through the full memory cell. The transmission of more than 53% for the visible wavelengths demonstrates that memory architecture with the selected materials can be used in several applications that require transparent devices.

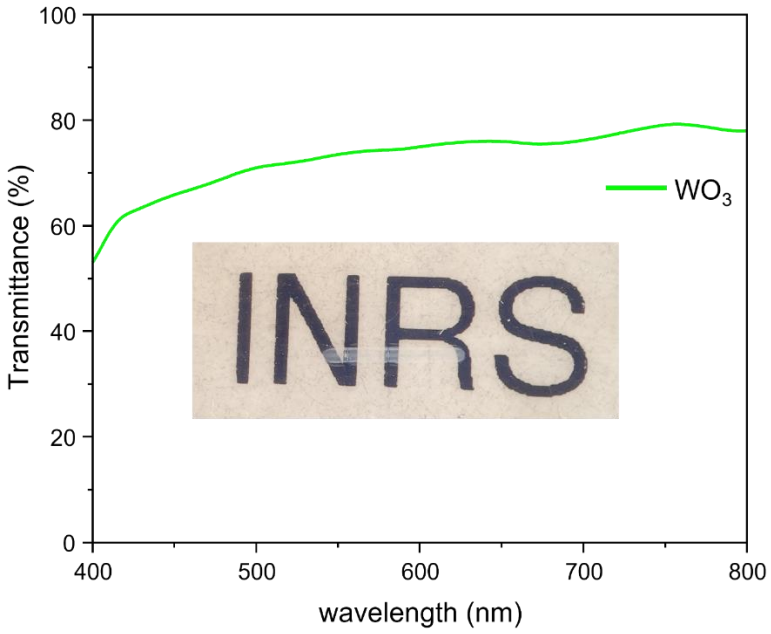

Figure 4.8: Transmittance characteristics of the full memory cells, the insert in the figure corresponds to an optical image of one of the devices and the transmitted logo of INRS. The spectral signature was taken at the location of a device and represents the added signatures of substrate and device.

4.2 PEDOT:PSS/ZnO/PEDOT:PSS Memory cells

Analog to the WO_3-based device described in section 4.1, the insulating layer within the MIM memory element now consists of ZnO sandwiched between PEDOT:PSS electrodes. The drop-on-demand process and parameters again follows section 3.1.1. The substrate is again flexible PEN foil.

4.2.1 Fabrication process

The PEDOT:PSS bottom electrode is 10 mm long, printed with 5 layers and a 25 μm drop space, resulting in a 200 μm wide electrodes. During the deposition of the insulating ZnO nanoparticles (Sigma-Aldrich H-SZ01034), this temperature is maintained. With a drop spacing of 10 μm, the middle 5 mm of PEDOT:PSS are covered with four layers of ZnO. Three top electrodes are placed perpendicular to the bottom electrode, with a length of 5 mm each, using the same parameters as the bottom electrode. To evaluate the effect of stress during bending cycles, the electrodes are positioned in the center and 1.5 mm to either side. Contacts for characterization are made easier by the vertical shift.

The temperature during the bottom electrode deposition is again kept at 60°C. Additionally, a 10 min drying step at 80°C is performed after deposition, to evaporate the residual solvents while leaving the bottom electrode and substrate unaffected. The ZnO is deposited at 80°C, and the top electrodes are deposited at 60°C, without the additional drying step.

4.2.2 X-ray diffraction measurements

The crystal structure of ZnO was investigated using four-circle X-ray diffraction with PANalytical X'pert Pro diffractometer equipped with a Cu $K\alpha_1$source. ($\lambda = 1.5406$ Å). From, the diffraction

pattern recorded in the range 30° - 80° was observed in Bragg-Brentano configuration (Θ-2Θ) with a 0.02° step size.

To investigate the degree of crystallinity of ZnO and obtain additional information about its crystal structure characteristics, X-ray diffraction experiments were done on the ZnO printed layer of the memory structure, as shown in figure 4.9. At room temperature, the deposited layer exhibited a polycrystalline structure with preferred orientations of (101) and (100). There were further diffraction peaks associated with the reflection of the (002), (102), (110), (103), (112), (201), (004), and (202) planes. The JCPDS card, No. 00-036-1451, was used to index all of the discovered diffraction peaks, indicating that the wurtzite structure was preserved despite the nanoparticles distributed in the ink. There are no substantial secondary phases or contaminants seen in the diffraction pattern.

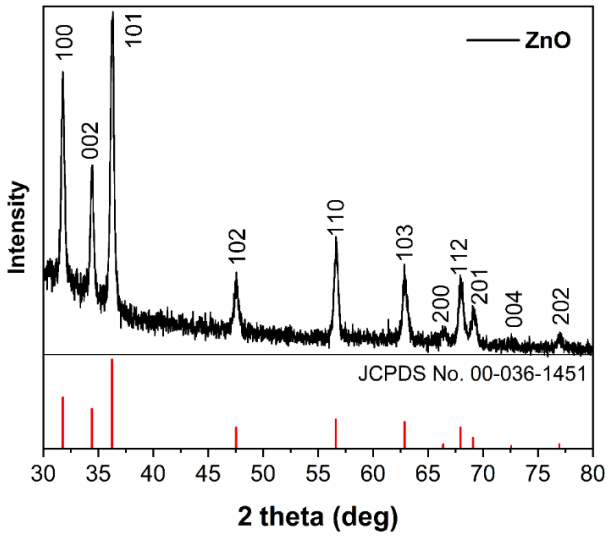

Figure 4.9: X-ray diffraction pattern of ZnO layer deposited at room temperature

4.2.3 Electrical Characterization

The electrical characterization follows section 3.2.2. The tungsten probes are directly contacted to the PEDOT:PSS bottom and top electrodes. The I-V curves are done using a voltage sweep from +5 V to -5 V with an increment of 0.01 V. The durability of the devices was evaluated by applying a pulsed switching sequence of +5 V/-5V write/erase pulses with a length of 0.1 s to record the resistances of the LRS (ON) and HRS (OFF) at a read voltage of +0.5 V for 10,000 cycles.

A schematic of the PEDOT: PSS/ZnO/PEDOT:PSS memory cell is shown in figure 4.10a. Figure 4.10b shows the memory device's current-voltage I(V) characteristic, as well as an inset of the I(V) characteristic on a semi-log scale. The top electrode was biased with a voltage of +5 V to 0 to -5 V to 0 and a compliance current (CC) of 100µA. while the bottom electrode was grounded. The memory cell switching behavior reveals the presence of a multilevel switching process in the positive sweep direction from HRS to LRS, with the LRS continuing in the negative sweep direction. A single-switching event from an LRS to an HRS is detected in the negative sweep direction, demonstrating non-volatile bipolar switching behavior. The estimated set voltage V_{set} is $\approx$ 0.7 V, whereas the reset voltage V_{reset} is $\approx$ 3.5 V in this case. The highest change in resistance for a sweep commencing in the positive direction occurs at around 0.7V, as seen in the inset of figure 4.10b. While a symmetric electrode design may imply a symmetric switching curve, there have been reports that the implicit electroforming during the initial switching cycle causes an asymmetry [107].

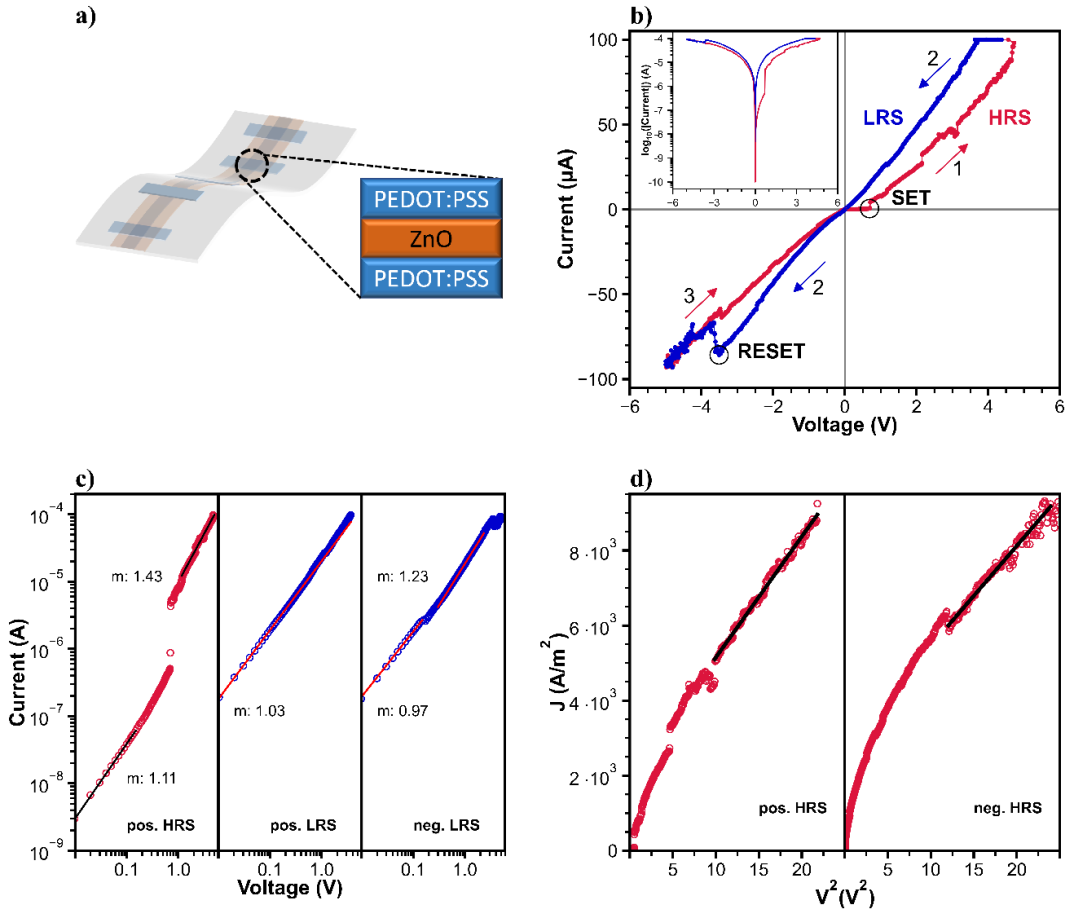

Figure 4.10: Current-voltage characteristics in PEDOT: PSS/ZnO/PEDOT: PSS memory (a) Schematic of the PEDOT: PSS/ZnO/PEDOT: PSS memory structure, (b) Current–Voltage characteristics of the corresponding memory cell in DC sweeping mode, (c) Experimental data (symbols) and linear fitting results (solid) of the positive HRS/LRS and negative LRS for the corresponding I(V) curve in log-log scale to determine conduction mechanism, (d) SCLC fitting plot of positive and negative HRS for high applied voltage range [108]**.**

The positive HRS/LRS and negative LRS are displayed in log-log scale to better understand the switching mechanism of the printed memory cell and to describe the electrical transport of the (PEDOT:PSS/ZnO/PEDOT:PSS) structure, as shown in figure 4.10c. The transition to the SET state can be seen in the positive HRS area, and a change in the conduction mechanism can be seen in the change in the slope *m* between 0.01 V and 0.15 V and between 1.2 V and 5.0 V, with m = 1.11 and 1.43, respectively. A linear fitting with a slope of around 1 was found prior to the SET and for small, applied bias, attesting for an Ohmic conduction regime. With further applied voltage, the

slope of the log(I)-log(V) changes again, abandoning the linear relationship, suggesting yet another conduction process to be explored later.

The development and transit of oxygen vacancies may be related to the resistive switching process in various oxide materials. The bulk or interfaces determine the conduction qualities of pristine ZnO, which is a weak conductor [17]. Sun et al. [109] revealed a screening effect, which may contribute to a proposed SCLC mechanism. The concentration of charge carriers at the electrode-dielectric interface prevents further charge carrier passage, reducing the amount of current that may flow [110]. Based on equation 4.3, the variation of J vs. V^2 was plotted in order to determine the primary transport mechanism at high applied bias, as shown in figure 4.10d. An excellent linear fitting of $J(V^2)$ is achieved after attaining a voltage of 3.13 V, showing that the SCLC model dominates the transport mechanism. The slope of the positive and negative LRS curves is used to establish the conduction mechanism, as shown in figure 4.10c. The positive LRS fits into a linear relationship with a slope of 1.03, indicating Ohmic conduction. The SET state stays Ohmic with a slope of 0.97 until an applied bias of 0.2 V when the applied voltage increases for the negative LRS curve. A shift in the slope is seen between 0.2 V and -3.51 V. This might be explained by the start of dissolving the oxygen vacancy filament when SCLC reaches its limit. Despite the device's SCLC limit, a RESET was seen, indicating that the applied electric field is powerful enough to thermally destroy the filament. When fitted with the SCLC model, the negative HRS curve that follows the negative LRS curve also has a linear behaviour, as seen in figure 4.10d, demonstrating the SCLC mechanism's prevalence. The filamentary route is not completely destroyed in this case, but it is severed from the electrode at the beginning and finish, leaving a build-up of oxygen vacancies in the ZnO layer.

The dielectric permittivity may be determined using the obtained fitting parameter to further assess the SCLC model's trustworthiness. Profilometry measurements (see section 3.2.3) were used to estimate the thickness d = 57 nm of a reference sample. The charge carrier mobility μ of

ZnO can be calculated using the nondegenerate semiconductor assumption $\sigma = e_0 n_o \mu$. [111][112].

For both positive and negative HRS, the conductivity σ can be determined using geometric dependencies and the lowest resistance value. Furthermore, because the trap-filled limit for positive and negative HRS has been exceeded, θ this estimation will be excluded. The SCLC fitting parameters and those of the density and mobility of free charge carriers were then used to determine the dielectric permittivity as shown in table 4.2: The estimated values of dielectric permittivity, free charge carrier mobility and density using the SCLC fitting parameter.

	$\boldsymbol{\varepsilon_r}$	$\boldsymbol{\mu}$ ($cm^2V^{-1}s^{-1}$)	$\boldsymbol{n_0}$ (cm^{-3})
positive HRS	8.53	$6.9 \cdot 10^{-6}$	10^{18}
negative HRS	7.50	$6.4 \cdot 10^{-6}$	10^{18}

Table 4.2: Summary of HRS properties

Although the values of μ are relatively low [111], the published value of free charge carrier density of $n_0 \approx 10^{18}\ cm^{-3}$ was utilised for the estimation of the dielectric permittivity [113]. The calculated ε_r value is in good agreement with the positive HRS value of 8.3 in comparison to the negative HRS, which ε_r value is smaller. The breakdown of the conductive filament causes oxygen vacancies to move against the electron flow, resulting in this discrepancy.

4.2.4 Mechanical Characterization

The effect of cyclic bending on the electrical performance of the (PEDOT:PSS/ZnO/PEDOT:PSS) memory cells was investigated using a rotate-to-bend home-made equipment [18]. The memory cell was held in place by two clamps on each side, one of which can rotate. The clamping distance, L is 6.45 mm, and the substrate thickness, *d* is 125 µm. A bending cycle is considered as a

symmetric flexure and compression of the memory cell with a maximum bending angle of 54°, resulting in a maximum bending radius, *r* of 3.1 mm, calculated using the equation 3.3 [91]:

The structure of this chapter is different from the previous one in terms of how you label sections and subsections. Please make this the same between both sections.

An I-V measurement is taken after a certain number of bending cycles to study the influence of cyclic bending on the electrical characteristics of the cells. To avoid the buildup of mechanical and electrical stress, electrical characterization is not conducted after each bending cycle. A voltage sweep is conducted in the same way as in the electrical characterization. At a read voltage of 0.5 V, the HRS and LRS are obtained from the ensuing I-V characteristics.

4.2.5 Conductive-AFM: Spreading resistance

Conductive atomic force microscopy (C-AFM) measurements were performed to allow for filament generation and to provide a verification of the local topography at the location of a filament in order to confirm filamentary switching and visualise field-induced conductive oxygen vacancy filament creation and desorption. The surface topography and current map of the pristine state of the ZnO layer are shown in figures 4.11a, and 4.11a'. Figure 4.11b shows a 9 V bias given to a 1µm x 1µm section of the layer, followed by a scan with a bias voltage of 1V. In comparison to the pure, unbiased surface regions, the corresponding current map (figure 4.11b') clearly shows a region with increased conductivity. The granular microstructure of nanosized grains is comparable in the biased and unbiased examined areas in figure 4.11b' and remains unchanged during the cell switching process. However, a considerable current contrast is shown in the current map acquired at the following values, suggesting a localised alteration attributable to the creation of the oxygen filament. Due to the clustering of oxygen vacancies in response to the applied electric field, a conductive filament appears as the bright spot on the current picture when a positive bias is applied. Reversing the polarity of the applied voltage causes the oxygen

filament to disintegrate (figure 4.11c'). This is a worthwhile difference to the same experiment in WO_3, in which the resistive switching process induced by the conductive AFM remained irreversible.

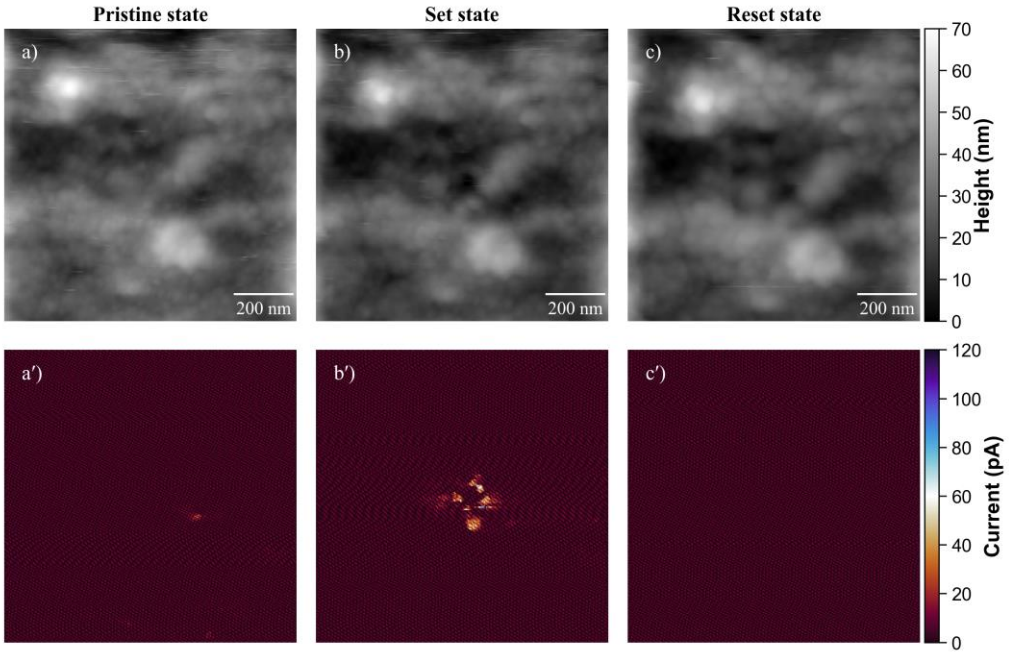

Figure 4.11: Topography images and their respective C-AFM current maps measured on 1x1µm² cell area by applying 1V at: (a-a') the pristine state, (b-b') after Set process: C-AFM current map shows the formation of the oxygen vacancy filament, and (c-c') Reset state and the disappearance of the conducting path. There is no significant change in topography throughout the switching events. The periodic noise on the current maps is due to 120 Hz noise coupled from building circuitry.

To assess the memory structures' stability and electrical performance, endurance and retention experiments on PEDOT:PSS/ZnO/PEDOT:PSS flexible transparent memory cells were carried out. Figures 4.12a, and 4.12b, respectively, show similar results. Pulse cycling was done 10^4 times with a voltage of ±5V for endurance measures, as shown in the inset of figure 4.12a. The ratio between HRS and LRS phases is roughly 5 during the cycling and remains consistent throughout 10^4 cycles. A pulse bias of 5 V for 0.5 s was used for retention measurements, resulting in a steady ratio between HRS and LRS up to $2.5x10^5$ s, as shown in figure 4.12b.

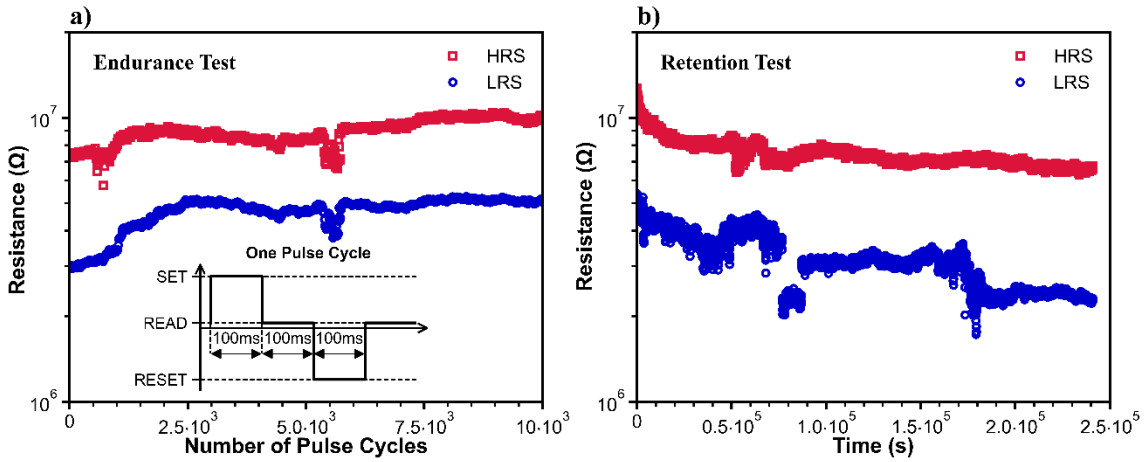

Figure 4.12: Endurance and retention of the PEDOT: PSS/ZnO/PEDOT:PSS cell (a) Endurance measured for 10^4 pulse cycles. The inset figure indicates the applied sequences of pulse with used measurement parameters (b) Retention characteristics of the PEDOT: PSS/ZnO/PEDOT:PSS flexible transparent memory cell performed at room temperature.

4.2.6 Bending-induced fatigue for the PEDOT:PSS/ZnO/PEDOT:PSS cell

For a single memory cell and a single bottom electrode line of different samples, the bending was done across numerous cycles ranging from pristine to 700 cycles, as shown in figure 4.13. The device stays completely operational up to 700 bending cycles with a bending radius of 3.1mm, according to the resistance measurement as a function of the bending cycles. Fitting a linear function to the Ohmic I-V yields the resistance of the single electrode line. The resistance of the single electrode line increases as the number of cycles increases. This attests to the reproducibility of the printing process as exactly the same performance was observed in the case of WO_3 devices and may again be explained by supposing that the substrate begins to fracture or splinter along the bending axis, deforming the electrode into several sections, as documented in Zardetto et al [106]. The resistance steadily increases, starting at 31.8 kΩ, until it reaches a point where the conduction along the PEDOT: PSS electrode breaks down, as it is a stepwise process. Due to the high deformation of the electrode material, the device maintains a consistent HRS/LRS

ratio as the number of bending cycles grows, but the total resistance values steadily increase. When bending approaches 700 cycles, the accompanying increase in resistance marks the start of the fatigue effect. Our mechanical fatigue analysis indicates that the performance degrades as a result of the electrodes' macroscopic failure rather than a problem with the resistive switching mechanism itself, given that the bending radius is orders of magnitudes larger than the diameter of the oxygen vacancy filament as determined by C-AFM. Further advances in the mechanical stability of flexible electrodes could result in a smaller resistance rise during long-term mechanical loading of our devices.

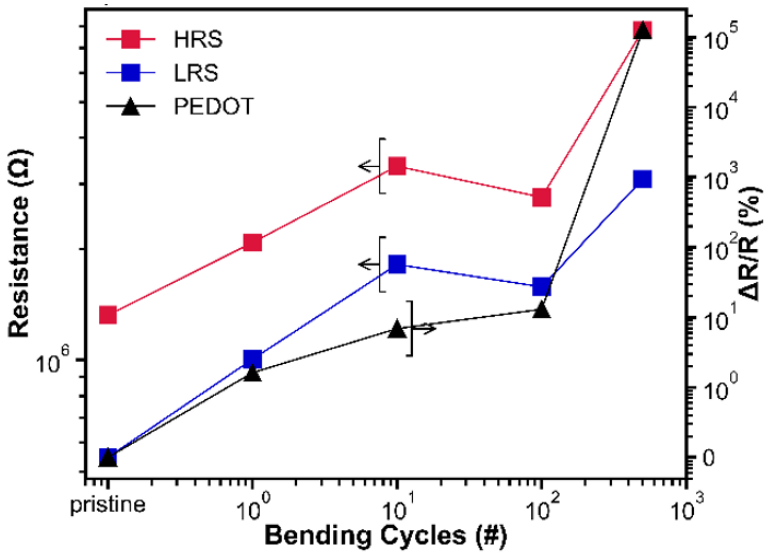

Figure 4.13: Bending performance evaluation of the flexible memory. The squares (in colors) represent the resistance values for HRS and LRS measured at 0.5V. The triangles denote the relative change in resistance measured for a PEDOT:PSS electrode. The arrows on the figure indicate the corresponding Y-axis.

4.2.7 Transmittance measurements of ZnO insulating layer

Transmittance spectra were collected on a Stellar Net BLUE-Wave (350-1150 nm) spectrometer linked to an Olympus BX41 microscope to analyze the device's optical features. The light source was a 100 W halogen lamp.

Figure 4.14 shows the transmittance of a full memory cell placed on a polyethylene naphthalate substrate. The figure's inset is an optical picture of one of the devices, with the label in the backdrop visible through the whole memory cell. The visible wavelength transmission of more than 86 % shows that memory architecture with the chosen materials may be employed in a variety of applications that need transparent devices.

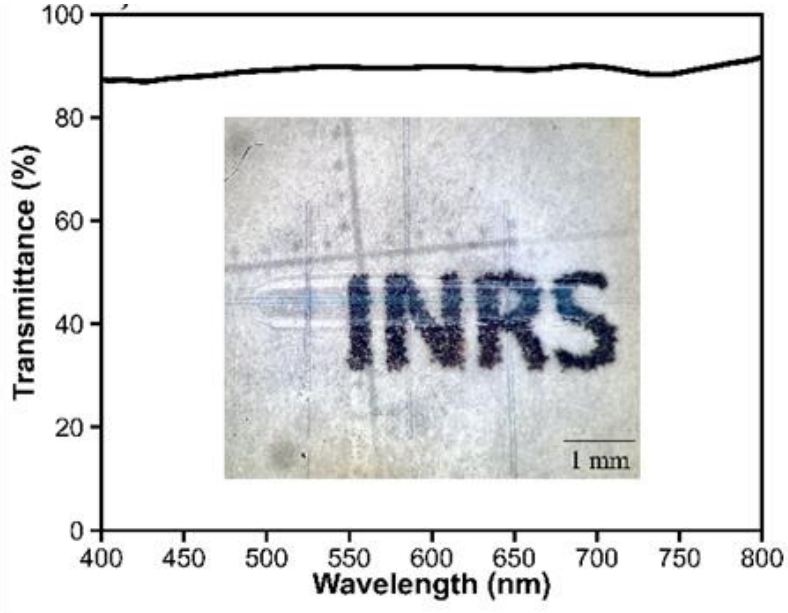

Figure 4.14: Transmittance characteristics of the full memory cells, the insert in the figure corresponds to an optical image of one of the devices and the transmitted logo of INRS

4.3 Comparison between WO_3 and ZnO

The direct comparison of WO_3 and ZnO needs to include a variety of parameters, not all of them necessarily related to the performance in the devices described above.[2] Whether or not a material has potential for printed ReRAM applications also relates to costs of the ink, handling of ink, toxicity, capability of recycling etc.

In terms of the latter, it should be noted that the polymeric substrate contributes by far the largest amount of material to the devices, followed by the polymeric electrodes and only then the oxide-based valency change material. So, in terms of circular economy, the devices under consideration are very much polymer items and will be treated as such.

With respect to toxicology, both WO_3 and ZnO in bulk phase are considered non-problematic unless digested. The same cannot be stated about nanoparticles, in particular nanoparticles of ZnO that were reported to be problematic for aquatic life [114]. However, ZnO, embedded in polymer matrices, is already widely used in e.g. food packaging due to a reported antibacterial effect [115] and the quantities released by this application are almost certainly exceeding the quantities that will ever be required for resistive RAM by several orders of magnitude.

Overall, albeit not perfectly safe, the risk assessment for the use of WO_3 and ZnO in resistive RAM applications does not indicate any substantial risks due to the low toxicity of the bulk phase, the encapsulation between polymeric electrodes plus an additional sandwich structure between the substrate and a laminated top layer to keep the devices in the zero-strain zone. This effectively prevents the formation of aerosols.

[2] With respect to the direct comparison of WO_3 and ZnO, we would like to remind the reader that the obvious material choice of a valency change ReRAM would have been TiO_2 and while this may still be an opportunity for future efforts, the attempts to ink-jet print TiO_2 layers with commercially available inks were not successful during this PhD project.

In terms of costs, the devices as discussed above have the advantage of only requiring two different inks, reducing the complexity of the printing setup and avoiding noble-metal inks. However, at present, the costs of inks are still mainly determined by the costs for research and development and the production of nanoparticles with narrow size distribution, keeping the advantage of material costs over other inks relatively low. Both inks allow for a sinter-free fabrication process with a maximum temperature of 60 degrees C associated to the deposition of the top- and bottom electrodes. This represents a substantial advantage over metal nanoparticle inks in CBRAM.

The direct comparison between WO_3 and ZnO should be made in the context of pure valency change switching. Earlier reports in literature about resistive switching in printed ZnO devices and until now, anything published on TiO_2-based devices, relates to CBRAM, so that previously reported ON/OFF ratios of three and more orders of magnitude should not be taken into consideration here. Table 4.3 represents the state of the art after the experiments of this PhD thesis.

	PEDOT:PSS/WO_3/PEDOT:PSS	PEDOT:PSS/ZnO/PEDOT:PSS
OFF resistivity (Ωcm)	$5.19X10^6$	$3.51X10^7$
ON/OFF ratio at read voltage	5.70	48.13
retention time (s)	80×10^3	2.5×10^5
endurance (cycles)	6000	10 000
transmission (visible wavelengths)	> 53%	> 86%
Bending cycles before failure	>700	>700

Table 4.3: Comparative summary between WO_3 and ZnO-based memory cells

As for the OFF resistivity, we see that for the case of ZnO, we achieve values that are $3.51x10^7$ Ωcm. For WO_3, the OFF resistivity is $5.19x10^6$ Ωcm, which is indicating stronger leakage contributions in what should otherwise be a comparable insulator. The somewhat lower

resistivity compared to bulk is attributed to a large amount of grain boundaries with electronic properties that substantially deviate from bulk [116][117].

As the ON resistance essentially depends on the nature of the filament, its electronic properties and the geometry, the error bars on these values are larger. One uncertainty originates from the speed at which the current compliance circuit is able to react, leaving uncertainties on the size of the filament.

As far as retention, fatigue resistance and optical transparency are concerned, ZnO appears to be superior to WO_3 in every single aspect. With a little reminder that the ZnO layer is thinner than the WO_3 layer, which affects the optical transmittance via Lambert-Beer's law, there may be room for improvement for the transparency of WO_3. This would however come at the expense of a lower OFF resistance. The number of possible switching cycles is also larger in ZnO (10,000) compared to WO_3 (6,000) and while both values are almost certainly far from the optimum that could be reached for even shorter switching pulses, there is a clear trend in favor of ZnO under otherwise similar conditions.

With respect to bending experiments, the number of bending cycles was not limited by either of the two oxide layers; in both cases, the devices failed due to crack formation in the polymeric electrodes and apparently neither of the two materials had a tangible effect on the mechanical properties of the electrodes.

Overall, the use of ZnO provides superior results in direct comparison to similar devices based on WO_3, which however remains a suitable material choice.

CHAPTER 5

5 SUMMARY AND OUTLOOK

Two different material choices for sintering free inkjet-printed bipolar VCM cells are presented in this thesis: WO_3 and ZnO. Both are deposited between transparent, symmetric PEDOT:PSS electrodes by inkjet printing. The fully printed memory cells as presented are suitable for applications in flexible electronics and shows first promising results for "Internet of Things" applications.

5.1 Summary

We demonstrated that the endurance of the device is stable for well above 10^4 cycles. The retention time for reliable information recovery was determined to be up to 28 hours, which currently limits the spectrum of possible applications. This retention time can almost certainly be improved by optimized read pulse durations that limit electrical strain on the devices and reduce the time-voltage dilemma (indicating that the read process is not entirely non-destructive [118]).

In order to build ReRAM devices, we examined the electrical performance, optical transmittance, and flexibility properties of WO_3 and ZnO-based inks. We found that the retention, endurance and optical transparency of ZnO cells are superior to WO_3 based devices (see Table 4.3).

We used flexible PEN foil as a substrate to print symmetric PEDOT:PSS/WO_3/PEDOT:PSS memory cells, which we used to perform bending tests. We show that for bending radii of 3.1 mm, the cell remains stable for 700 bending cycles for both materials. The failure behavior was traced back to the PEDOT:PSS-electrodes that started to exhibit cracks.

We demonstrated that reproducible switching characteristics can be achieved without sintering and electroforming. We identified the migration of oxygen vacancies across the cell as the dominant underlying resistance switching mechanism. Multiple conduction mechanisms involving oxygen vacancies exist in both media, which we comparatively fitted to the current-voltage characteristics for both devices. We found that the HRS is dominated by the SCLC conduction mechanism whereas the LRS confirmed the oxygen vacancy filament-mediated process with a linear I-V relationship in both materials.

The device characteristics, as far as the material properties are concerned, are similar to the clean room produced counterparts. Additive manufacturing of resistively switching memory cells based on either WO_3 or ZnO is therefore feasible with any technique providing sufficiently thin structures to allow for the formation of oxygen vacancy filament formation, in particular ink-jet printing.

5.2 Outlook

Based on the results of this thesis, there are a couple of technological and scientific questions that deserve additional attention in the future, some of them of more immediate interest, some others of more fundamental concern.

As for the technological, short-term goals, it is certainly worthwhile pursuing the quest for a TiO_2-based device. Titanium dioxide has been widely investigated as active material in resistively switching memory cells and a substantial amount of material science knowledge could be readily transferred from clean room fabricated devices to the generation of printed cells.

A second item related to materials refers to the stability of PEDOT:PSS electrodes to bending. Given that the mechanical resistance of our devices was clearly limited by the mechanical stability

of the electrodes, it is a worthwhile consideration to either modify the mechanical properties of the deposited PEDOT:PSS electrodes via e.g. additives or to consider replacing them with e.g. carb on nanotube based inks.

These process-related items also indicate that the results presented in this thesis are a proof of concept for sinter-free printed valency-change memory and that the results reported here, as encouraging as they appear, are almost certainly far from what may be achievable in terms of retention and fatigue resistance for a dedicated optimization study. Future studies should also address the thermal stability of these devices.

ReRAM offers the opportunity to tune the ON state by appropriate choice of e.g. the current compliance and/or the pulse height and width of the write pulse. This provides the opportunity for neuromorphic computing in which the state of the memory cell can we gradually changed between ON and OFF, providing switching characteristics described through spike-time-dependent-plasticity that resemble those of synapses and that provide an opportunity for weighted resistances in a crossbar-based neural network.

REFERENCES

[1] Y. Bonnassieux *et al.*, "The 2021 flexible and printed electronics roadmap," *Flex. Print. Electron.*, vol. 6, no. 2, 2021, doi: 10.1088/2058-8585/abf986.

[2] "The Largest Capacity Flash Drives Currently Available | Digital Trends." https://www.digitaltrends.com/computing/largest-flash-drives/ (accessed Sep. 12, 2022).

[3] "At 100TB, the world's biggest SSD gets an (eye-watering) price tag | TechRadar." https://www.techradar.com/news/at-100tb-the-worlds-biggest-ssd-gets-an-eye-watering-price-tag (accessed Sep. 12, 2022).

[4] R. Waser, R. Dittmann, C. Staikov, and K. Szot, "Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, no. 25–26, pp. 2632–2663, 2009, doi: 10.1002/adma.200900375.

[5] KBV Research, "Global Printed Electronics Market Size, Share & Industry Trends Analysis Report By Material, By Technology, By Device, By Regional Outlook and Forecast, 2022 – 2028," 2022. doi: 6289282.

[6] L. Wu, Z. Dong, F. Li, H. Zhou, and Y. Song, "Emerging Progress of Inkjet Technology in Printing Optical Materials," *Adv. Opt. Mater.*, vol. 4, no. 12, pp. 1915–1932, 2016, doi: 10.1002/adom.201600466.

[7] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet printing-process and its applications," *Adv. Mater.*, 2010, doi: 10.1002/adma.200901141.

[8] M. Jung *et al.*, "All-Printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 571–580, 2010, doi: 10.1109/TED.2009.2039541.

[9] A. M. Gaikwad, D. A. Steingart, T. Nga Ng, D. E. Schwartz, and G. L. Whiting, "A flexible high potential printed battery for powering printed electronics," *Appl. Phys. Lett.*, vol. 102, no. 23, 2013, doi: 10.1063/1.4810974.

[10] N. Sani *et al.*, "All-printed diode operating at 1.6 GHz," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 111, no. 33, pp. 11943–11948, 2014, doi: 10.1073/pnas.1401676111.

[11] M. Kang *et al.*, "Synergistic High Charge-Storage Capacity for Multi-level Flexible Organic Flash Memory," *Sci. Rep.*, vol. 5, pp. 1–9, 2015, doi: 10.1038/srep12299.

[12] S. Majumdar, B. Chen, Q. H. Qin, H. S. Majumdar, and S. van Dijken, "Electrode Dependence of Tunneling Electroresistance and Switching Stability in Organic Ferroelectric P(VDF-TrFE)-Based Tunnel Junctions," *Adv. Funct. Mater.*, vol. 28, no. 15, pp. 1–8, 2018, doi: 10.1002/adfm.201703273.

[13] Z. Lü, T. Pu, Y. Huang, X. Meng, and H. Xu, "Flexible ferroelectric polymer devices based on inkjet-printed electrodes from nanosilver ink," *Nanotechnology*, vol. 26, no. 5, 2015, doi: 10.1088/0957-4484/26/5/055202.

[14] S. Zou and C. Michael, "Flexible non-volatile Cu/CuxO/Ag ReRAM memory devices fabricated using ink-jet printing technology," *Proc. - Electron. Components Technol. Conf.*, pp. 441–446, 2014, doi: 10.1109/ECTC.2014.6897321.

[15] P. Vilmi *et al.*, "Fully printed memristors for a self-sustainable recorder of mechanical

energy," *Flex. Print. Electron.*, vol. 1, no. 2, 2016, doi: 10.1088/2058-8585/1/2/025002.
[16] G. Vescio *et al.*, "Inkjet printed HfO_2-based ReRAMs: First demonstration and performance characterization," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 457–460, 2017, doi: 10.1109/LED.2017.2668599.
[17] F. C. Chiu, "A review on conduction mechanisms in dielectric films," *Advances in Materials Science and Engineering*. 2014, doi: 10.1155/2014/578168.
[18] S. Ali, J. Bae, C. H. Lee, K. H. Choi, and Y. H. Doh, "All-printed and highly stable organic resistive switching device based on graphene quantum dots and polyvinylpyrrolidone composite," *Org. Electron.*, vol. 25, pp. 225–231, 2015, doi: 10.1016/j.orgel.2015.06.040.
[19] S. Nau *et al.*, "Inkjet-printed resistive switching memory based on organic dielectric materials: From single elements to array technology," *Adv. Electron. Mater.*, vol. 1, no. 1–2, pp. 1–6, 2015, doi: 10.1002/aelm.201400003.
[20] B. Huber, P. B. Popp, M. Kaiser, A. Ruediger, and C. Schindler, "Fully inkjet printed flexible resistive memory," *Appl. Phys. Lett.*, vol. 110, no. 14, 2017, doi: 10.1063/1.4978664.
[21] H. Gao, J. Li, F. Zhang, Y. Liu, and J. Leng, "Materials Horizons," 2019, doi: 10.1039/c8mh01070f.
[22] T. Carey *et al.*, "electronics," *Nat. Commun.*, doi: 10.1038/s41467-017-01210-2.
[23] "IEEE Roadmaps Guide Future Memories & Applications." https://www.forbes.com/sites/tomcoughlin/2018/11/29/ieee-roadmaps-guide-future-memories-applications/?sh=6b2d3d74689f (accessed Sep. 14, 2022).
[24] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," *Proc. IEEE*, vol. 91, no. 4, pp. 489–501, 2003, doi: 10.1109/JPROC.2003.811702.
[25] W. Wan *et al.*, "A compute-in-memory chip based on resistive random-access memory," *Nature*, vol. 608, no. 7923, pp. 504–512, 2022, doi: 10.1038/s41586-022-04992-8.
[26] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, "Recent progress in resistive random access memories: Materials, switching mechanisms, and performance," *Materials Science and Engineering R: Reports*. 2014, doi: 10.1016/j.mser.2014.06.002.
[27] I. S. Devised *et al.*, "I NTERNATIONAL T ECHNOLOGY R OADMAP FOR 2011 E DITION P ROCESS I NTEGRATION , D EVICES , AND," 2011.
[28] V. Garcia and M. Bibes, "Ferroelectric tunnel junctions for information storage and processing," *Nat. Commun.*, vol. 5, 2014, doi: 10.1038/ncomms5289.
[29] Z. Wen, C. Li, D. Wu, A. Li, and N. Ming, "Ferroelectric-field-effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions," *Nat. Mater.*, vol. 12, no. 7, pp. 617–621, 2013, doi: 10.1038/nmat3649.
[30] O. Auciello and J. F. Scott, "THE PHYSICS OF to save the document on your," no. December 2015, 1998, doi: 10.1063/1.882324.
[31] G. Grynkewich *et al.*, "N onvolatile Magnetoresistive Magnetic Tunnel Junctions," no. November, 2004.
[32] A. Physics, "Toward a Universal Memory," no. April, pp. 508–511, 2005.
[33] M. Le Gallo and A. Sebastian, "An overview of phase-change memory device physics," *J. Phys. D. Appl. Phys.*, vol. 53, no. 21, 2020, doi: 10.1088/1361-6463/ab7794.
[34] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nanosci.*

Technol. A Collect. Rev. from Nat. Journals, pp. 158–165, 2009, doi: 10.1142/9789814287005_0016.

[35] F. Zahoor, T. Z. Azni Zulkifli, and F. A. Khanday, "Resistive Random Access Memory (RRAM): an Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications," *Nanoscale Res. Lett.*, vol. 15, no. 1, 2020, doi: 10.1186/s11671-020-03299-9.

[36] J. S. Lee, S. Lee, and T. W. Noh, "Resistive switching phenomena: A review of statistical physics approaches," *Appl. Phys. Rev.*, vol. 2, no. 3, 2015, doi: 10.1063/1.4929512.

[37] A. Sawa, "Resistive switching in transition metal oxides," *Mater. Today*, vol. 11, no. 6, pp. 28–36, 2008, doi: 10.1016/S1369-7021(08)70119-6.

[38] D. Ielmini and R. Waser, *Resistive Switching From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications*. Germany: Wiley-VCH Verlag, 2016.

[39] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Erratum: Electrochemical metallization memories - Fundamentals, applications, prospects (Nanotechnology (2011) 22 (254003))," *Nanotechnology*, vol. 22, no. 28, 2011, doi: 10.1088/0957-4484/22/28/289502.

[40] B. Mittermeier, "Inkjet-printed Flexible Resistive Switching Memory," INRS, University of Quebec, 2019.

[41] S. Tsui *et al.*, "Field-induced resistive switching in metal-oxide interfaces," *Appl. Phys. Lett.*, vol. 85, no. 2, pp. 317–319, 2004, doi: 10.1063/1.1768305.

[42] X. Chen *et al.*, "Nonvolatile bipolar resistance switching effects in multiferroic $BiFeO_3$ thin films on $LaNiO_3$-electrodized Si substrates," *Appl. Phys. A Mater. Sci. Process.*, vol. 100, no. 4, pp. 987–990, 2010, doi: 10.1007/s00339-010-5910-y.

[43] C. Mannequin *et al.*, "Stress-induced leakage current and trap generation in HfO_2 thin films," *J. Appl. Phys.*, vol. 112, no. 7, 2012, doi: 10.1063/1.4756993.

[44] B. Gao *et al.*, "Unified Physical Model of Bipolar Oxide-Based Resistive Switching Memory," vol. 30, no. 12, pp. 1326–1328, 2009.

[45] A. You, M. A. Y. Be, and I. In, "Stability of the interface between indium-tin- poly (styrenesulfonate) in polymer light- emitting diodes," *Appl. Phys. Lett.*, vol. 2255, no. 2000, 2002.

[46] P. Peumans and S. R. Forrest, "Very-high-efficiency double-heterostructure copper phthalocyanine/C60 photovoltaic cells," *Appl. Phys. Lett.*, vol. 79, no. 1, pp. 126–128, 2001, doi: 10.1063/1.1384001.

[47] B. G. Horowitz, "Organic Field-Effect Transistors," no. 5, pp. 365–377, 1998.

[48] A. M. Nardes *et al.*, "Microscopic understanding of the anisotropic conductivity of PEDOT:PSS thin films," *Adv. Mater.*, vol. 19, no. 9, pp. 1196–1200, 2007, doi: 10.1002/adma.200602575.

[49] S. R. Dupont, F. Novoa, E. Voroshazi, and R. H. Dauskardt, "Decohesion kinetics of PEDOT:PSS conducting polymer films," *Adv. Funct. Mater.*, vol. 24, no. 9, pp. 1325–1332, 2014, doi: 10.1002/adfm.201302174.

[50] A. Lenz, H. Kariis, A. Pohl, P. Persson, and L. Ojamäe, "The electronic structure and reflectivity of PEDOT:PSS from density functional theory," *Chem. Phys.*, vol. 384, no. 1–3, pp. 44–51, 2011, doi: 10.1016/j.chemphys.2011.05.003.

[51] F. Gunkel, D. V. Christensen, Y. Z. Chen, and N. Pryds, “Oxygen vacancies: The (in)visible friend of oxide electronics,” *Appl. Phys. Lett.*, vol. 116, no. 12, 2020, doi: 10.1063/1.5143309.

[52] M. Gillet, K. Aguir, C. Lemire, E. Gillet, and K. Schierbaum, “The structure and electrical conductivity of vacuum-annealed WO_3 thin films,” *Thin Solid Films*, 2004, doi: 10.1016/j.tsf.2004.04.018.

[53] A. You, M. A. Y. Be, and I. In, “Structural transformation induced changes in the optical properties of nanocrystalline tungsten oxide thin films,” vol. 171903, no. April 2010, pp. 1–4, 2016, doi: 10.1063/1.3421540.

[54] Y. Yao, D. Sang, L. Zou, Q. Wang, and C. Liu, “A Review on the Properties and Applications of WO_3 Nanostructure − Based Optical and Electronic Devices,” 2021.

[55] A. Phys, “Variable-temperature Raman spectroscopic study of the hydrogen sensing mechanism in Pt-WO_3 nanowire film,” vol. 113104, no. January, 2013, doi: 10.1063/1.4798280.

[56] M. A. Gondal, M. A. Dastageer, and A. Khalil, “Synthesis of nano-WO_3 and its catalytic activity for enhanced antimicrobial process for water purification using laser induced photo-catalysis,” *Catal. Commun.*, 2009, doi: 10.1016/j.catcom.2009.10.011.

[57] P. S. Patil, S. H. Mujawar, A. I. Inamdar, P. S. Shinde, H. P. Deshmukh, and S. B. Sadale, “Structural, electrical and optical properties of TiO_2 doped WO_3 thin films,” *Appl. Surf. Sci.*, 2005, doi: 10.1016/j.apsusc.2005.03.074.

[58] S. B. Uni, “Ferroelectric WO_3 Nanoparticles for Acetone Selective Detection,” no. 7, pp. 4794–4796, 2008.

[59] S. K. Gullapalli, R. S. Vemuri, and C. V. Ramana, “Structural transformation induced changes in the optical properties of nanocrystalline tungsten oxide thin films,” *Appl. Phys. Lett.*, 2010, doi: 10.1063/1.3421540.

[60] J. Kim *et al.*, “Effect of Electronegativity on Bipolar Resistive Switching in a WO_3-Based Asymmetric Capacitor Structure,” *ACS Appl. Mater. Interfaces*, 2016, doi: 10.1021/acsami.5b11781.

[61] S. Lee, K. H. Yun, and D. Kim, “Electroforming-less and multi-level resistive switching characteristics in tungsten oxide thin film,” *Thin Solid Films*, 2019, doi: 10.1016/j.tsf.2019.02.012.

[62] Y. T. Li *et al.*, “Investigation of resistive switching behaviours in WO_3-based RRAM devices,” *Chinese Phys. B*, vol. 20, no. 1, 2011, doi: 10.1088/1674-1056/20/1/017305.

[63] K. Ellmer, A. Klein, and B. Rech, “Transparent Conductive Zinc Oxide,” *Inorg. Mater.*, vol. 104, no. 3, pp. 79–124, 2008, doi: 10.1007/978-3-540-73612-7.

[64] F. C. Chiu, P. W. Li, and W. Y. Chang, “Reliability characteristics and conduction mechanisms in resistive switching memory devices using ZnO thin films,” *Nanoscale Res. Lett.*, vol. 7, pp. 1–9, 2012, doi: 10.1186/1556-276X-7-178.

[65] C. N. Peng *et al.*, “Resistive switching of Au/ZnO/Au resistive memory: An in situ observation of conductive bridge formation,” *Nanoscale Res. Lett.*, vol. 7, pp. 1–6, 2012, doi: 10.1186/1556-276X-7-559.

[66] F. M. Simanjuntak, D. Panda, K. H. Wei, and T. Y. Tseng, “Status and Prospects of ZnO-

Based Resistive Switching Memory Devices," *Nanoscale Res. Lett.*, vol. 11, no. 1, 2016, doi: 10.1186/s11671-016-1570-y.

[67] M. Laurenti, S. Porro, C. F. Pirri, C. Ricciardi, and A. Chiolerio, "Zinc Oxide Thin Films for Memristive Devices: A Review," *http://dx.doi.org/10.1080/10408436.2016.1192988*, vol. 42, no. 2, pp. 153–172, Mar. 2016, doi: 10.1080/10408436.2016.1192988.

[68] R. H. Bishop, *The mechatronics handbook*. 2002.

[69] M. J. Uddin, J. Hassan, and D. Douroumis, "Thermal Inkjet Printing: Prospects and Applications in the Development of Medicine," *Technologies*, vol. 10, no. 5, p. 108, 2022, doi: 10.3390/technologies10050108.

[70] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet printing-process and its applications," *Adv. Mater.*, vol. 22, no. 6, pp. 673–685, 2010, doi: 10.1002/adma.200901141.

[71] "Numerical calculation of the fluid dynamics of drop-on-demand jets | IBM Journal of Research and Development." https://dl.acm.org/doi/abs/10.1147/rd.283.0322 (accessed Aug. 01, 2022).

[72] D. B. van Dam and C. Le Clerc, "Experimental study of the impact of an ink-jet printed droplet on a solid substrate," *Phys. Fluids*, vol. 16, no. 9, p. 3403, Aug. 2004, doi: 10.1063/1.1773551.

[73] N. Reis, C. Ainsley, and B. Derby, "Ink-jet delivery of particle suspensions by piezoelectric droplet ejectors," *J. Appl. Phys.*, vol. 97, no. 9, pp. 8–14, 2005, doi: 10.1063/1.1888026.

[74] J. G. Korvink, P. J. Smith, and D. Y. Shin, "Inkjet-based micromanufacturing," *Inkjet-based Micromanufacturing*, pp. 1–371, May 2012, doi: 10.1002/9783527647101.

[75] E. Tekin, P. J. Smith, and U. S. Schubert, "Inkjet printing as a deposition and patterning tool for polymers and inorganic particles," *Soft Matter*, vol. 4, no. 4, pp. 703–713, 2008, doi: 10.1039/b711984d.

[76] E. Tekin, B. J. De Gans, and U. S. Schubert, "Ink-jet printing of polymers - From single dots to thin film libraries," *J. Mater. Chem.*, vol. 14, no. 17, pp. 2627–2632, 2004, doi: 10.1039/b407478e.

[77] J. G. (Jan G. . Korvink, P. J. (Mechanical engineer) Smith, and D.-Y. Shin, "Inkjet-based micromanufacturing," p. 371, 2012.

[78] P. Buffat and J. P. Borel, "Size effect on the melting temperature of gold particles," *Phys. Rev. A*, vol. 13, no. 6, pp. 2287–2298, 1976, doi: 10.1103/PhysRevA.13.2287.

[79] J. R. Greer and R. A. Street, "Thermal cure effects on electrical performance of nanoparticle silver inks," *Acta Mater.*, vol. 55, no. 18, pp. 6345–6349, 2007, doi: 10.1016/j.actamat.2007.07.040.

[80] J. Niittynen, E. Sowade, H. Kang, R. R. Baumann, and M. Mäntysalo, "Comparison of laser and intense pulsed light sintering (IPL) for inkjet-printed copper nanoparticle layers," *Sci. Rep.*, vol. 5, 2015, doi: 10.1038/SREP08832.

[81] J. Perelaer, B. J. De Gans, and U. S. Schubert, "Ink-jet printing and microwave sintering of conductive silver tracks," *Adv. Mater.*, vol. 18, no. 16, pp. 2101–2104, Aug. 2006, doi: 10.1002/ADMA.200502422.

[82] M. L. Allen *et al.*, "Electrical sintering of nanoparticle structures," *Nanotechnology*, vol. 19, no. 17, p. 175201, Apr. 2008, doi: 10.1088/0957-4484/19/17/175201.

[83] Y. Kim *et al.*, “Memristor crossbar array for binarized neural networks,” *AIP Adv.*, vol. 9, no. 4, pp. 7–12, 2019, doi: 10.1063/1.5092177.

[84] M. Lee *et al.*, “High Density Resistance RAM Applications,” *Electron Devices Meet. 2007. IEDM 2007. IEEE Int.*, pp. 771–774, 2007.

[85] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, “Complementary resistive switches for passive nanocrossbar memories,” *Nat. Mater.*, vol. 9, no. 5, pp. 403–406, 2010, doi: 10.1038/nmat2748.

[86] M. P. Murrell *et al.*, “Spatially resolved electrical measurements of SiO_2 gate oxides using atomic force microscopy,” *Appl. Phys. Lett.*, vol. 62, no. 7, pp. 786–788, 1993, doi: 10.1063/1.108579.

[87] K. D. Harris, A. L. Elias, and H. J. Chung, “Flexible electronics under strain: a review of mechanical characterization and durability enhancement strategies,” *J. Mater. Sci.*, vol. 51, no. 6, pp. 2771–2805, 2016, doi: 10.1007/s10853-015-9643-3.

[88] J. Lewis, “Material challenge for flexible organic devices,” *Mater. Today*, vol. 9, no. 4, pp. 38–45, 2006, doi: 10.1016/S1369-7021(06)71446-8.

[89] D. R. Cairns and G. P. Crawford, “Electromechanical properties of transparent conducting substrates for flexible electronic displays,” *Proc. IEEE*, vol. 93, no. 8, pp. 1451–1458, 2005, doi: 10.1109/JPROC.2005.851515.

[90] O. Glushko, M. J. Cordill, A. Klug, and E. J. W. List-Kratochvil, “The effect of bending loading conditions on the reliability of inkjet printed and evaporated silver metallization on polymer substrates,” *Microelectron. Reliab.*, vol. 56, pp. 109–113, 2016, doi: 10.1016/j.microrel.2015.10.007.

[91] B. Huber, J. Schober, M. Kaiser, A. Ruediger, and C. Schindler, “Rotate-to-bend setup for fatigue bending tests on inkjet-printed silver lines,” *Flex. Print. Electron.*, vol. 3, no. 3, 2018, doi: 10.1088/2058-8585/aad5a4.

[92] S. Il Park, J. H. Ahn, X. Feng, S. Wang, Y. Huang, and J. A. Rogers, “Theoretical and experimental studies of bending of inorganic electronic materials on plastic substrates,” *Adv. Funct. Mater.*, vol. 18, no. 18, pp. 2673–2684, 2008, doi: 10.1002/adfm.200800306.

[93] M. Delfag, R. Katoch, J. Jehn, Y. Gonzalez, C. Schindler, and A. Ruediger, “Sinter-free inkjet-printed PEDOT:PSS/WO_3/PEDOT:PSS flexible valency change memory,” *Flex. Print. Electron.*, vol. 6, no. 3, p. 035011, Sep. 2021, doi: 10.1088/2058-8585/ac1fd7.

[94] F.-C. Chiu, “A Review on Conduction Mechanisms in Dielectric Films,” *Adv. Mater. Sci. Eng.*, vol. 2014, pp. 1–18, Mar. 2014, doi: 10.1155/2014/578168.

[95] M. A. Lampert, “Currents in an Insulator with Traps J =,” vol. 1, 1956.

[96] D. F. Barbe, “Space-charge-limited current enhanced by Frenkel effect,” *J. Phys. D. Appl. Phys.*, vol. 4, no. 11, pp. 1812–1815, 1971, doi: 10.1088/0022-3727/4/11/427.

[97] A. Donnadieu, D. Davazoglou, and A. Abdellaoui, “Structure, optical and electro-optical properties of polycrystalline WO_3 and MoO_3 thin films prepared by chemical vapour deposition,” *Thin Solid Films*, vol. 164, no. C, pp. 333–338, Oct. 1988, doi: 10.1016/0040-6090(88)90158-7.

[98] G. Zheng, J. Wang, H. Liu, and V. Murugadoss, “Tungsten oxide nanostructures and nanocomposites for photoelectrochemical water splitting,” vol. 18968, pp. 18968–18994,

2019, doi: 10.1039/c9nr03474a.

[99] J. S. Lee, S. Lee, and T. W. Noh, “Resistive switching phenomena: A review of statistical physics approaches,” *Applied Physics Reviews*. 2015, doi: 10.1063/1.4929512.

[100] S. Lee, J. S. Lee, J. B. Park, Y. K. Kyoung, M. J. Lee, and T. W. Noh, “Anomalous effect due to oxygen vacancy accumulation below the electrode in bipolar resistance switching Pt/Nb:$SrTiO_3$ cells,” *APL Mater.*, vol. 2, no. 6, 2014, doi: 10.1063/1.4884215.

[101] K. McKenna and A. Shluger, “The interaction of oxygen vacancies with grain boundaries in monoclinic HfO_2,” *Appl. Phys. Lett.*, 2009, doi: 10.1063/1.3271184.

[102] C. Ferreyra, W. Román Acevedo, R. Gay, D. Rubi, and M. J. Sánchez, “Oxygen vacancy dynamics in redox-based interfaces: Tailoring the memristive response,” *J. Phys. D. Appl. Phys.*, vol. 53, no. 1, 2020, doi: 10.1088/1361-6463/ab46d3.

[103] Y. S. Lin *et al.*, “Resistive switching mechanisms relating to oxygen vacancies migration in both interfaces in Ti/HfOx/Pt memory devices,” *J. Appl. Phys.*, vol. 113, no. 6, 2013, doi: 10.1063/1.4791695.

[104] G. Catalan, “Magnetocapacitance without magnetoelectric coupling,” *Appl. Phys. Lett.*, vol. 88, no. 10, 2006, doi: 10.1063/1.2177543.

[105] D. J. Dimaria and E. Cartier, “Mechanism for stress-induced leakage currents in thin silicon dioxide films,” *J. Appl. Phys.*, 1995, doi: 10.1063/1.359905.

[106] V. Zardetto, T. M. Brown, A. Reale, and A. Di Carlo, “Substrates for flexible electronics: A practical investigation on the electrical, film flexibility, optical, temperature, and solvent resistance properties,” *J. Polym. Sci. Part B Polym. Phys.*, vol. 49, no. 9, pp. 638–648, May 2011, doi: 10.1002/POLB.22227.

[107] “WO2013040714A1.pdf.” .

[108] M. Delfag, G. Rachovitis, Y. González, J. Jehn, and A. H. Youssef, “Fully printed ZnO-based valency-change memories for flexible and transparent applications OPEN ACCESS Fully printed ZnO-based valency-change memories for flexible and transparent applications.”

[109] Y. Sun *et al.*, “Effect of carrier screening on ZnO-based resistive switching memory devices,” *Nano Res.*, vol. 10, no. 1, pp. 77–86, 2017, doi: 10.1007/s12274-016-1267-7.

[110] E. W. Lim and R. Ismail, “Conduction mechanism of valence change resistive switching memory: A survey,” *Electron.*, vol. 4, no. 3, pp. 586–613, 2015, doi: 10.3390/electronics4030586.

[111] S. Bubel, N. Mechau, H. Hahn, and R. Schmechel, “Trap states and space charge limited current in dispersion processed zinc oxide thin films Trap states and space charge limited current in dispersion processed zinc,” no. February 2014, 2010, doi: 10.1063/1.3524184.

[112] A. Rockett, “The materials science of semiconductors,” *Mater. Sci. Semicond.*, pp. 1–622, 2008, doi: 10.1007/978-0-387-68650-9/COVER.

[113] S. A. Studenikin, N. Golego, and M. Cocivera, “Carrier mobility and density contributions to photoconductivity transients in polycrystalline ZnO films,” *J. Appl. Phys.*, vol. 87, no. 5, pp. 2413–2421, 2000, doi: 10.1063/1.372194.

[114] J. Liu, X. Feng, L. Wei, L. Chen, B. Song, and L. Shao, “The toxicology of ion-shedding zinc oxide nanoparticles,” *http://dx.doi.org/10.3109/10408444.2015.1137864*, vol. 46, no. 4, pp. 348–384, Apr. 2016, doi: 10.3109/10408444.2015.1137864.

[115] P. J. P. Espitia, C. G. Otoni, and N. F. F. Soares, “Zinc Oxide Nanoparticles for Food Packaging

Applications," *Antimicrob. Food Packag.*, pp. 425–431, Jan. 2016, doi: 10.1016/B978-0-12-800723-5.00034-6.

[116] M. Regragui, V. Jousseaume, M. Addou, A. Outzourhit, J. C. Bernéde, and B. El Idrissi, "Electrical and optical properties of WO_3 thin films," *Thin Solid Films*, vol. 397, no. 1–2, pp. 238–243, 2001, doi: 10.1016/S0040-6090(01)01405-5.

[117] T. Asokan and R. Freer, "Grain and grain boundary conduction in zinc oxide varistors before and after DC degradation," *J. Eur. Ceram. Soc.*, vol. 11, no. 6, pp. 545–550, Jan. 1993, doi: 10.1016/0955-2219(93)90114-7.

[118] P. Huang *et al.*, "Analysis of the voltage-time dilemma of metal oxide-based rram and solution exploration of high speed and low voltage ac switching," *IEEE Trans. Nanotechnol.*, vol. 13, no. 6, pp. 1127–1132, 2014, doi: 10.1109/TNANO.2014.2340571.

APPENDIX

A.1 Waveforms for Inkjet Inks

The waveforms that were utilised to print on the various materials are described in this appendix. The Dimatix DMP2832 printer's DMC-11610 cartridge, which has a nozzle diameter of LN = 21 µm, is used to print all the materials.

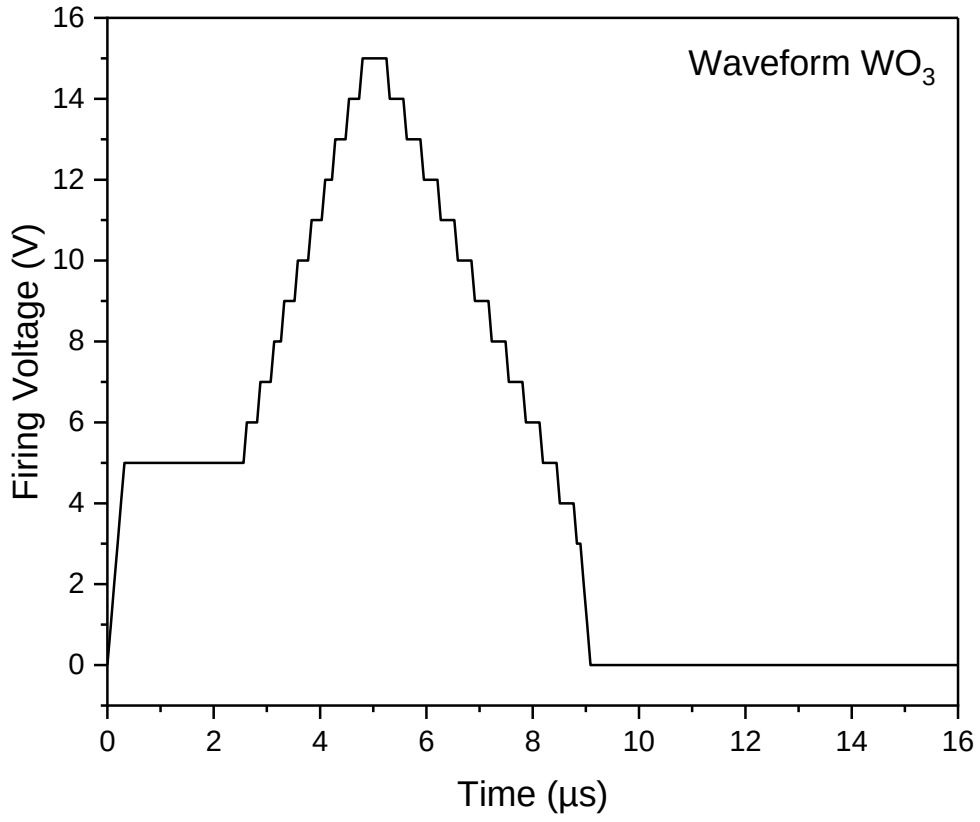

Figure A.1 Waveform for WO_3 nanoparticles ink with a maximum voltage of 15 V.

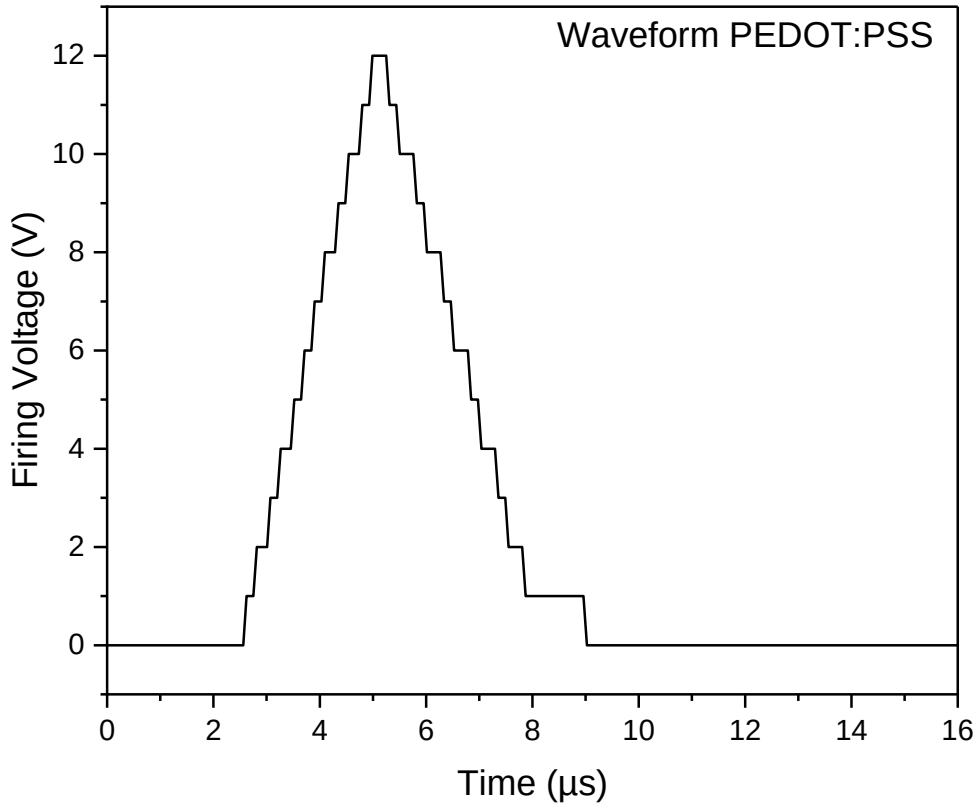

Figure A.2 Waveform for PEDOT:PSS nanoparticles ink with maximum voltage of 12V.

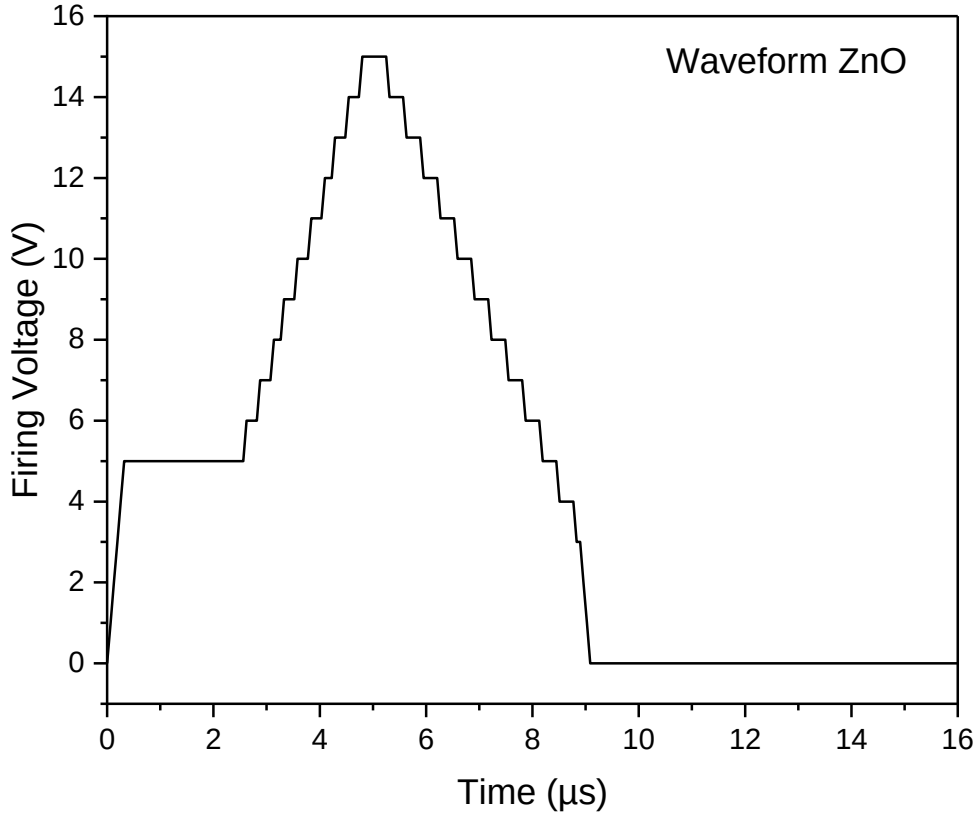

Figure A.3 waveform for ZnO nanoparticles ink with maxima voltage of 15V.

A.2 Publications and Conference Contributions

Significant portions of this thesis have already been presented at conferences or published as journal papers. The following is a list of conference presentations and published papers.

Publications

- M. Delfag, R. Katoch, J. Jehn, Y. Gonzalez, C. Schindler, and A. Ruediger, "Sinter-free inkjet-printed PEDOT:PSS/WO3/PEDOT:PSS flexible valency change memory," *Flex. Print. Electron.*, vol. 6, no. 3, p. 035011, Sep. 2021, doi: 10.1088/2058-8585/ac1fd7.
- M. Delfag, G. Rachovitis, Y. González, J. Jehn, and A. H. Youssef, "Fully printed ZnO-based valency-change memories for flexible and transparent applications OPEN ACCESS Fully printed ZnO-based valency-change memories for flexible and transparent applications."

Conference Contributions

- Poster: Mohamed Delfag, Rajesh Katoch, Johannes Jehn, Yoandris Gonzalez, Christina Schindler and Andreas Ruediger, Sintering-free inkjet-printed PEDOT:PSS/WO_3/PEDOT:PSS flexible valency change memory. *XXIX INTERNATIONAL MATERIALS RESEARCH CONGRESS, Cancun, Mexico, 2021.*
- Talk: Mohamed Delfag, Rajesh Katoch, Yoandris Gonzalez, Johannes Jehn, Christina Schindler and Andreas Ruediger, Sinter-free inkjet-printed PEDOT:PSS/WO_3/PEDOT:PSS flexible valency change memory. *Nanotechnology Materials and Devices Conference (NMDC), IEEE. Vancouver, BC, Canada, 2021.*

SOMMAIRE RÉCAPITULATIF

Mémoire flexible à changement de valence imprimée par jet d'encre sans frittage

Introduction

Les nouvelles applications des technologies de l'information et de la communication, telles que la vidéo haute définition (HD), le divertissement multimédia et les services de données et d'information, continuent de pénétrer le marché des consommateurs avec des performances et une complexité croissante. Toutes ces nouvelles applications nécessitent le stockage de grandes quantités de données, dont une partie au moins est stockée localement. Cela se traduit par une demande croissante de stockage d'informations, ce qui place les dispositifs de mémoire parmi les actifs les plus critiques du marché de l'électronique. En ce qui concerne les solutions portables, il est déjà possible de stocker 1 To [1] de données dans des dispositifs de mémoire flash (clé USB) disponibles dans le commerce et la capacité totale des disques durs des ordinateurs portables atteint même aujourd'hui 100 To [2]. En outre, ces dispositifs de stockage conservent les données sans alimentation électrique, ce qui signifie qu'ils sont non volatils. Pour être compétitifs en tant que mémoire, ces dispositifs doivent présenter des caractéristiques telles que la non-volatilité, une capacité élevée, une réponse rapide en lecture/écriture et en effacement, une faible consommation d'énergie et une grande endurance [3].

De nos jours, la principale technologie où la non-volatilité est perceptible est la technologie dite "flash". Sa conception est basée sur un transistor à effet de champ métal-oxyde-semi-conducteur (MOSFET) avec une grille flottante où sont stockées des charges pour moduler la tension de seuil. La structure d'une mémoire flash est relativement simple, et c'est cette simplicité, associée à d'excellentes propriétés de rétention des données, qui a rendu les mémoires flash si populaires

aujourd'hui. Cependant, la miniaturisation continue des MOSFET n'est pas sans poser de problèmes. Par exemple, une épaisseur d'oxyde tunnel inférieure à 16 nm peut entraîner des conséquences indésirables, telles qu'une perte de données et un courant de fuite très élevé. Par conséquent, le concept de mémoire flash est actuellement confronté à des problèmes sérieux de mise à l'échelle [4]. Malgré toutes ces avancées vers une densité d'intégration toujours plus élevée des dispositifs de mémoire, diverses applications exigent des caractéristiques supplémentaires telles que la flexibilité et la transparence optique, mais au détriment de la capacité de stockage. La nécessité de disposer d'installations de salles blanches de pointe pour la production des transistors mentionné ci-dessus est incompatible avec la production au point d'utilisation où une capacité de mémoire relativement faible est suffisante.

Parmi les exemples possibles, citons les tickets de transport public qui contiennent des informations sur les utilisations multiples, les étiquettes intelligentes qui suivent, par exemple, la température ou d'autres paramètres externes pendant le transport : la liste ne cesse de s'allonger au fur et à mesure que les possibilités de production au point d'utilisation évoluent. Une technique que nous connaissons tous pour produire des documents et des photos de haute qualité sans avoir besoin d'une presse dédiée, est l'impression. Si les premières imprimantes à aiguilles ont rapidement été remplacées par des imprimantes à jet d'encre, puis par des imprimantes laser, la liberté de produire des documents de haute qualité à tout moment reste un pilier de la gestion des bureaux dans le monde entier. Et si cette liberté de produire des unités de haute qualité en quantité relativement faible pouvait être étendue des documents aux circuits électroniques avec les fonctionnalités respectives ? Cela a déjà été réalisé dans une large mesure pour les écrans et il y a une demande croissante pour pousser vers le marché les composants complémentaires des circuits électroniques, y compris la logique et la mémoire. De 2018 à 2025, le marché mondial de l'électronique imprimée devrait connaître un taux de croissance annuel composé de plus de 11 %, pour atteindre 17,26 milliards USD. Les tendances significatives du marché comprennent la pénétration accrue de l'Internet des objets, l'évolution de la technologie d'impression numérique, la réduction des coûts de production, le besoin de substrats durables

et flexibles pour générer de l'électronique imprimée sécurisée, et les technologies écologiques [5].

Développements récents et état de l'art

L'électronique imprimée possède déjà la maturité technologique nécessaire pour fabriquer la plupart des composants requis à l'aide de techniques d'impression. Sur des substrats transparents et minces, avec des tailles et des conceptions extrêmement précises adaptées à l'architecture de mémoire crossbar, l'impression à jet d'encre a été utilisée avec succès et a même démontré des flux de processus sans frittage avec des électrodes et des matériaux diélectriques [6].

Aujourd'hui, chaque élément de circuit, y compris l'unité de mémoire, peut être imprimé pour évoluer vers des circuits entièrement imprimés. En particulier, dans le cas des applications de mémoire, l'impression convient à la fabrication de mémoire à accès aléatoire résistives (Resistive Random Access Memory : ReRAM) puisqu'elle ne nécessite qu'une structure métal-isolant-métal (MIM) relativement simple avec une taille de cellule minimale de $4F^2$, où F est la taille minimale des caractéristiques déterminée par le procédé de fabrication. Pour permettre la logique binaire, l'unité de mémoire fondamentale de toute nouvelle technologie de mémoire, également appelée cellule de mémoire, doit être commutable entre au moins les deux états logiques "0" et "1". Les états logiques sont définis par la résistance de la cellule de mémoire : un état de haute résistance (High resistance state: HRS) correspond à "0" et un état de basse résistance (Low resistance state: LRS) correspond à "1". "RAM résistive" est un nom descriptif puisque les états logiques sont déterminés par la résistance de la cellule de mémoire.

La ReRAM à pont conducteur et à changement de valence est particulièrement attrayante pour l'impression en raison de sa construction simple à trois couches combinée à des tensions de fonctionnement potentiellement faibles. Cela a entraîné une augmentation du nombre de

publications sur les dispositifs ReRAM imprimés au cours des dernières années. Différentes architectures et combinaisons de matériaux sont étudiées, ainsi que des combinaisons de différentes technologies d'impression et de cellules partiellement imprimées.

Types de mémoire à accès aléatoire

Les mémoires sont un composant majeur de la microélectronique. Son importance peut être corrélée au développement de l'électronique portable (téléphones cellulaires, ordinateurs portables, etc.), qui nécessite des capacités de stockage toujours plus grandes. Le stockage d'informations peut être divisé en deux catégories selon le type de mémoire, volatile ou non volatile. En particulier pour les applications mobiles, où l'énergie est limitée, la mémoire non volatile présente l'avantage indéniable de prolonger la durée de fonctionnement avec une seule charge de batterie. Les mémoires volatiles comprennent plusieurs conceptions de mémoire qui, dans tous les cas, nécessitent une alimentation électrique continue pour maintenir les informations stockées.

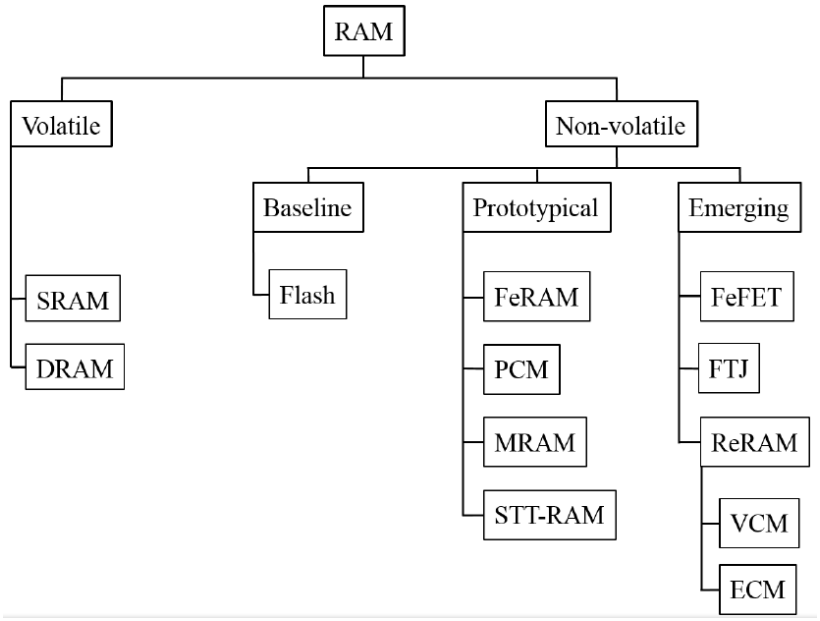

Figure 2.1 : Une classification des nombreuses technologies de RAM qui ne présente que les types les plus importants. Selon le niveau de développement technologique, la RAM non volatile est classée en trois catégories : mémoire de base, prototype et mémoire émergente [23].

Mémoire à accès aléatoire résistive bipolaire (ReRAM) :

La mémoire à accès aléatoire résistive bipolaire (ReRAM) fonctionne en modifiant de manière réversible la résistance d'un matériau diélectrique par inversion de polarisation, contrairement à la PCRAM qui fonctionne avec différentes durées et amplitudes de la même polarisation. Une cellule ReRAM a une structure très simple. Il s'agit d'un dispositif métal-isolant-métal (MIM).

Une ReRAM est basée sur le fait que certaines structures MIM présentent un changement de résistance (ou transition résistive) suite à l'application d'une tension. Initialement, la structure MIM a une résistance élevée ((HRS), ou état OFF). Lorsque la différence de potentiel aux bornes de la structure est augmentée, à une certaine valeur de tension, le dispositif passe à l'état conducteur, également appelé état de faible résistance ((LRS) ou état ON). Dans des conditions appropriées, le dispositif peut ensuite être ramené à l'état d'isolation. La commutation entre les états OFF et ON se fait en appliquant une certaine tension de polarité opposée (mode "bipolaire", le plus général, figure 2.3b). Dans certains cas, il est possible de revenir à un état isolant en appliquant une tension de même polarité (mode "unipolaire", figure 2.3a) [34]. Le cycle isolant-conducteur-isolant peut être répété presque indéfiniment tant que le dispositif est stable [35]. On a donc une structure à deux niveaux de résistance (isolant/conducteur), avec la possibilité de passer de l'un à l'autre par simple application d'une tension : ces dispositifs peuvent être utilisés pour créer des mémoires non volatiles réinscriptibles. Cela rend les dispositifs ReRAM très attractifs et beaucoup moins limités en termes de miniaturisation [36].

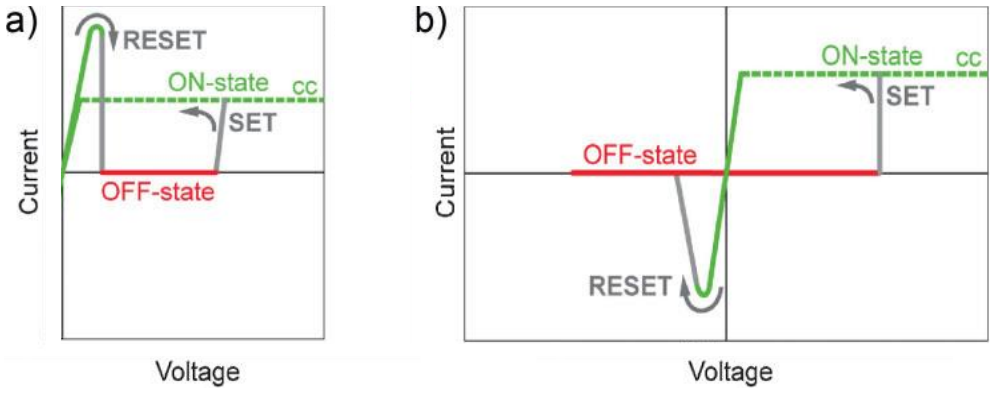

Figure 2.3 : Les deux systèmes de fonctionnement fondamentaux des cellules de mémoire utilisant la commutation résistive. Courbes I-V enregistrées pour un signal de tension de forme triangulaire [3].

Mécanisme de commutation résistif dans la ReRAM:

Migration des cations métalliques à partir de l'anode (mémoires résistives de type CBRAM)

Les cations qui sont formés par oxydation électrochimique au niveau d'une anode électrochimiquement active (par exemple, argent, or, cuivre) migrent vers la cathode chargée négativement pour y être réduits et déposés. La croissance ultérieure d'un filament donnera alors lieu à un chemin conducteur à travers la couche isolante. Le système MIM est composé (i) d'une anode qui est un métal " électrochimiquement actif ", c'est-à-dire capable de fournir des cations qui seront injectés dans l'oxyde (électrode dite " active ") ; (ii) d'une couche isolante qui est un espaceur passif et poreux entre les deux électrodes permettant la dérive et/ou la diffusion des ions métalliques ; (iii) d'une cathode constituée d'un métal " inerte ", c'est-à-dire qui ne fournit aucun cation à l'oxyde (électrode dite " inerte "). Le processus SET débute à l'interface anode/oxyde, où les atomes de l'anode sont oxydés et injectés dans l'oxyde. Sous l'action du champ, ces cations métalliques vont migrer vers la cathode. Une fois que les cations métalliques atteignent la cathode (électrode inerte), ils vont capturer des électrons et ainsi se réduire (électro-cristallisation) pour former un pont conducteur. Une fois le pont formé, formant un

court-circuit entre les électrodes, la tension s'effondre et arrête la croissance d'autres dendrites qui auraient pu se développer en parallèle - un scénario du type "le gagnant rafle tout". Pendant la croissance du filament métallique, le potentiel du filament est celui de la cathode, ce qui empêche son oxydation (dissolution). Ainsi, pendant la SET, le filament croît de l'électrode inerte (cathode) vers l'électrode active (anode). Lorsque le filament atteint l'anode, le dispositif passe à l'état ON [38]. Comme le montre la figure 2.5. Après avoir inversé la polarité de la tension appliquée, l'électrode inerte devient anode, et l'électrode active devient cathode. En augmentant la différence de potentiel au-delà d'une certaine valeur (VRESET), le filament métallique sera à nouveau oxydé et dissous dans l'isolant. En raison de la forme conique du filament, la résistance du cône métallique est plus élevée au sommet.

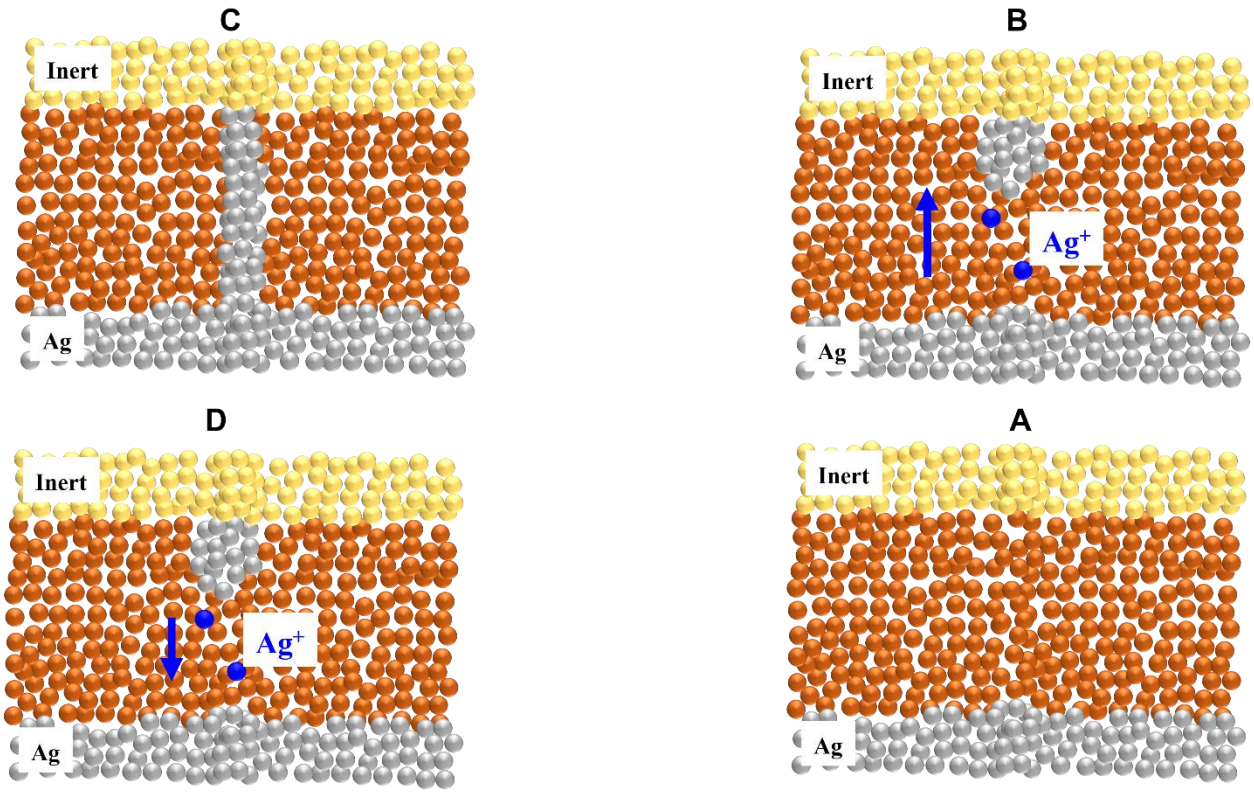

Figure 2.4: Commutation bipolaire de la mémoire ECM: (A) développement du filament dans l'état OFF à haute résistance, (B) croissance du filament (C), état ON à basse résistance, (D) dissolution du filament dans l'état de tension inversée. Adapté de [40].

C'est donc à ce point que le gradient de potentiel (le champ électrique) est le plus élevé. C'est donc au sommet du cône que la dissolution est initiée. Pendant la phase RESET, le filament va se rétracter de l'électrode active (nouvelle cathode) vers l'électrode inerte (nouvelle anode). Ainsi, les atomes précédemment impliqués dans le processus de SET seront récupérés par l'électrode active (nouvelle cathode) et l'état OFF est restauré [3]. En général, une fois que le filament est généré lors d'une étape initiale d'électroformage, l'opération suivante est beaucoup plus rapide car elle ne concerne que l'ouverture et la fermeture de l'espace entre le filament et la cathode. Les changements typiques de résistance entre l'état OFF isolant et l'état ON métallique sont de l'ordre de quatre à six ordres de grandeur.

Mécanismes de changement de valence:

Filaments de vacance d'oxygène

Dans de nombreux oxydes, notamment les oxydes de métaux de transition, les lacunes d'oxygène sont facilement formées ou annihilées par l'échange d'oxygène avec l'atmosphère ambiante. Pour des raisons de neutralité de charge, les lacunes en oxygène portent une charge nominale de -2, étant donné que l'oxygène qui occupait précédemment le site était dans un état de valence 2- mais a quitté l'échantillon sous forme d'oxygène moléculaire et donc de charge neutre. Cette charge de -2 implique que les lacunes d'oxygène sont sensibles au champ électrique externe et dériveront sous une polarisation externe. Les structures ZnO- et WO_3 sont deux représentants de structures qui présentent une semi-conduction importante pour des concentrations courantes de lacunes d'oxygène, tout en étant des isolants dans leur structure stœchiométrique. Dans ce cas, la commutation de résistance est souvent attribuée à la création de vacances d'oxygène agrégées dans l'oxyde. Sous polarisation, des lacunes d'oxygène sont générées dans l'oxyde (réactions d'oxydoréduction à l'anode ou rupture des liaisons métal-oxygène sous l'effet d'électrons énergétiques) [3]. Dans le même temps, des ions oxygène (O^{2-}) sont créés. Les ions oxygène migrent vers l'anode, tandis que les vacances d'oxygène (chargées positivement, V_O^{z+}) migrent vers la cathode. En atteignant l'anode, les ions oxygène perdent leurs électrons en excès,

ce qui peut conduire à la libération d'oxygène gazeux ou à l'oxydation de l'anode. A la cathode, les électrons seront injectés sur les lacunes d'oxygène (niveaux donneurs ionisés, V_O^{z+}) et pourront atteindre l'anode par des mécanismes de saut entre les lacunes. Un courant circule donc dans le dispositif (état ON). Ainsi, on considère que les chemins de conduction dans l'oxyde sont composés de lacunes d'oxygène [42] (figure 2.6) ou, de la même manière, qu'ils sont composés de phases d'oxygène sous-stoechiométriques ayant une conductivité plus élevée que la phase stoechiométrique. C'est donc la génération de lacunes d'oxygène qui joue un rôle primordial dans le comportement de ces oxydes métalliques. Cette classe de ReRAMs, basée sur la présence de vacances d'oxygène (et d'ions oxygène), définit les mémoires résistives de type OxRAM (Oxygen based ReRAM). Les changements typiques de résistance dans une cellule OxRAM entre l'état initial isolant OFF et l'état semi-conducteur ON sont de l'ordre d'un à deux ordres de grandeur, donc quelque peu inférieurs aux changements entre un état isolant OFF et un état métallique ON dans la CBRAM. Cependant, comme dans le CBRAM, le filament est une résistance parallèle à la couche isolante, tandis que l'effet d'interface discuté ci-dessus représente une résistance en série.

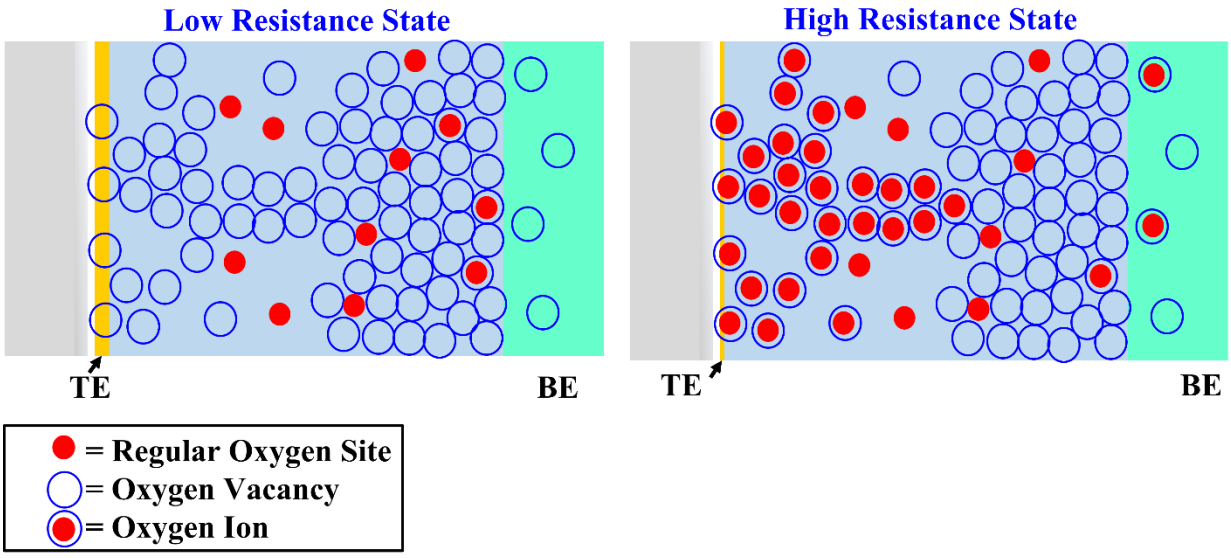

Figure 2.6 : La formation (destruction) du filament conducteur constitué de lacunes d'oxygène. BE et TE désignent respectivement les électrodes inférieure et supérieure.

FABRICATION D'UN DISPOSITIF À JET D'ENCRE

Pour l'impression à jet d'encre par gouttelettes, l'encre est acheminée depuis un réservoir à travers une ouverture de l'ordre du micron (buse) via un actionneur piézoélectrique. Le matériau piézoélectrique se déforme lorsqu'une impulsion de tension est appliquée, et une gouttelette d'encre est éjectée de la buse (voir figure 3.1).

L'impulsion de tension peut être ajustée pour s'adapter à une large gamme de viscosités et de tensions de surface de l'encre. L'encre est une solution ou une dispersion de matériau fonctionnel dans un solvant. Les nanoparticules métalliques, les polymères conducteurs et non conducteurs, les isolants et les composés photo-chimiquement actifs sont des exemples de composants d'encre fonctionnels [67].

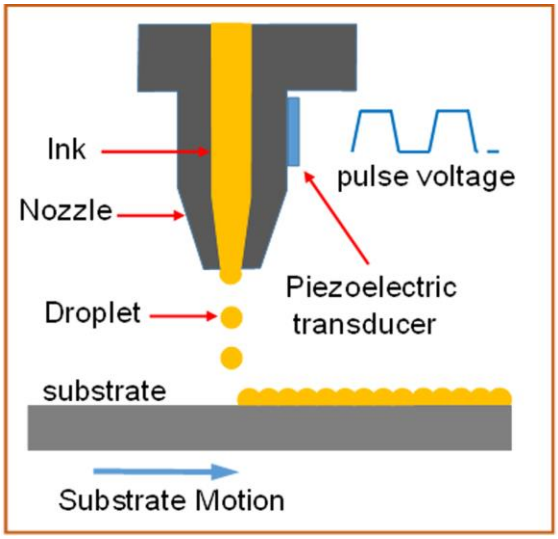

Figure 3.1 : Schéma du processus d'impression à jet d'encre: un actionneur piézoélectrique est placé près du canal d'encre et de la buse [69].

L'impression à jet d'encre est simple, rapide, peu coûteuse et polyvalente. De petits volumes de liquide, de l'ordre du pico-litre, sont déposés avec une précision de l'ordre du micromètre. Les caractéristiques typiques sont de 10 à 50 µm. Si le dépôt de gouttelettes individuelles est rapide, il ne convient pas pour couvrir de grandes surfaces. L'impression sur des substrats souples

permet de réaliser des produits électroniques flexibles, contrairement à la structure rigide de la technologie des semi-conducteurs.

s, ainsi que des taux d'évaporation accrus [68] et des combinaisons de solvants [69] peuvent être utilisés pour limiter l'effet de tache de café.

$$Z = \frac{\sqrt{D\sigma\rho}}{\eta} \qquad (3.1)$$

Où D est le diamètre de la buse, ρ est la densité de l'encre, σ est sa tension superficielle et η sa viscosité dynamique. La plage appropriée pour l'impression à jet d'encre par gouttes à la demande est comprise entre 1 et 10. Pour un Z plus petit, la viscosité élevée de l'encre empêche souvent l'éjection des gouttelettes. Pour un Z plus élevé, une quantité croissante de gouttelettes satellites accompagne la gouttelette primaire [70]. Les encres utilisées dans ce travail ont les nombres Z suivants : Z=1.0 (PEDOT : PSS), Z=2.1 (ZnO) et Z=7.4 (WO_3), calculés avec un diamètre de buse D=21 µm.

Le rayon d'étalement de la goutte d'encre est déterminé par l'énergie de surface du substrat et l'interaction encre-substrat, décrite par la théorie de la mouillabilité. Des traitements chimiques ou au plasma peuvent être utilisés pour ajuster la mouillabilité du substrat. Par exemple, le traitement au plasma d'oxygène améliore les caractéristiques hydrophiles d'un substrat. Par conséquent, une encre non polaire s'étendra moins sur un substrat traité au plasma d'oxygène, mais une encre polaire s'étendra davantage.

Motif de gouttelettes

Un motif de gouttes est imprimé sur un substrat pour concevoir une forme spécifique, qui se chevauchent et forment la structure. L'espacement des gouttes, ou l'espace entre les gouttes sur le substrat, est un aspect critique de la qualité d'impression et doit être modifié en fonction des caractéristiques de l'encre et de l'interaction avec le substrat. Si l'espacement des gouttes est trop important, les gouttes sur le substrat ont moins de chances de se chevaucher, ce qui entraîne des lacunes dans la structure. Si l'espacement des gouttes est trop faible, trop de matériau sera déposé, ce qui entraînera un renflement de la structure [71]. Par conséquent, l'espacement des gouttes doit être ajusté pour chaque combinaison particulière d'encre et de substrat.

Effet de tache de café

L'effet dit de tache de café décrit la tendance des matières dissoutes à se déposer près de la périphérie de la structure. À la frange de la structure, où la ligne de contact (ménisque) entre l'encre et le substrat est épinglée, le taux d'évaporation du solvant est plus important dès que la gouttelette d'encre mouille le substrat. Par conséquent, la matière s'écoule du centre vers la périphérie, ce qui entraîne une plus grande quantité de matière déposée à la périphérie et une plus grande taille de l'élément structurel à la périphérie. Une faible concentration de solvant et de grandes viscosité.

RÉSULTATS ET DISCUSSION

Cette section résume notre étude des cellules de mémoire ReRAM imprimées par jet d'encre. Le ZnO et le WO_3 sont étudiés dans des structures MIM, en utilisant des matériaux d'électrode transparents PEDOT:PSS pour former des cellules de mémoire. Le substrat de base est une feuille flexible de polyéthylène naphtalate (PEN). Les caractéristiques du dispositif sont présentées, en

utilisant les techniques de caractérisation suivantes : Microscopie à force atomique, microscopie électronique, caractérisation IV, ainsi qu'un montage de flexion sur mesure.

Cellules de mémoire PEDOT:PSS/WO_3/PEDOT:PSS

Processus de fabrication

L'électrode inférieure en PEDOT:PSS est imprimée en utilisant un espacement des gouttes est de 25 µm. La largeur de l'électrode est de ∼200 µm. L'impression de 5 couches permet d'obtenir une épaisseur d'environ 150-200 nm. Ensuite, l'encre à nanoparticules WO_3 est imprimée avec un espacement des gouttes de 5 µm comme couche isolante. Une pile de 8 couches est imprimée sur le dessus du PEDOT:PSS. Enfin, l'électrode supérieure est déposée à l'identique de l'électrode inférieure, perpendiculairement à cette dernière pour former la structure en croix. L'espacement des gouttes et le nombre de couches pour le PEDOT:PSS sont le résultat d'un processus d'optimisation visant à obtenir une conductivité élevée et reproductible pour un film le plus fin possible, tandis que la même optimisation pour la couche de WO_3 visait une épaisseur suffisante pour éviter les fuites entre l'électrode supérieure et l'électrode inférieure à travers la couche poreuse de nanoparticules. Pendant le processus d'impression, des températures de 60°C et 30°C ont été maintenues pour les électrodes et l'oxyde.

Caractéristiques courant-tension lors de la commutation résistive

Des mesures électriques quasi-statiques avec un pas de tension de 10 mV et des balayages de tension entre 4.5 V et -4.5 V ont été effectuées. Aucune procédure d'électroformage séparée n'a été nécessaire pour activer les cellules de mémoire.

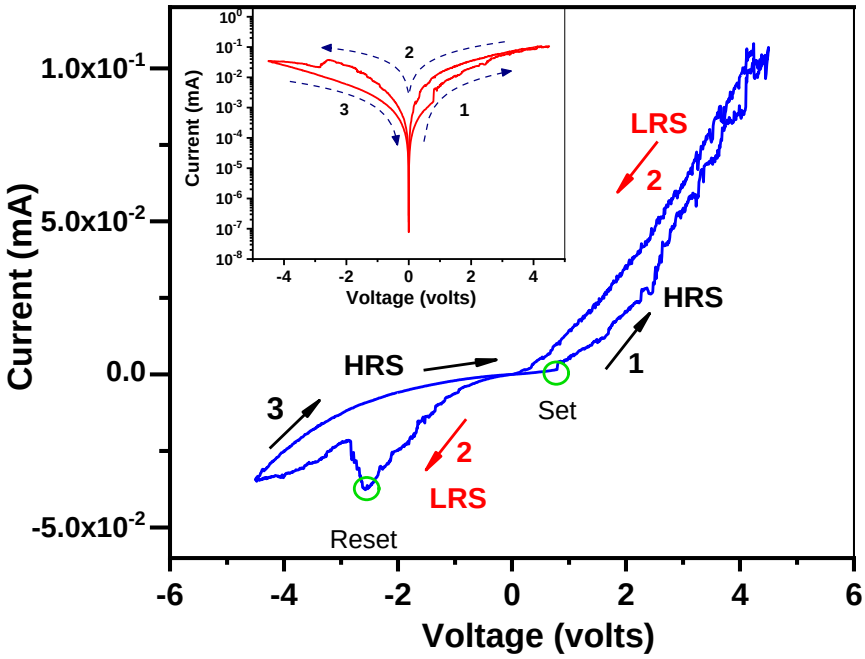

Figure 4.4: Courbe de commutation I-V typique enregistrée sur une cellule PEDOT:PSS/WO3/PEDOT:PSS. L'encart montre la valeur absolue du courant sur une échelle semi-logarithmique. La commutation est caractérisée par deux comportements de commutation distincts : i) commutation analogique de l'état HRS (1) à l'état LRS (2) dans le cycle positif ; et ii) commutation analogique de réinitialisation de l'état LRS (2) à l'état HRS (3) dans le cycle négatif.

Le balayage quasi-statique consistait en des mesures électriques individuelles le long d'un profil de tension en dents de scie. On observe que les cellules passent de l'état OFF à haute résistance à l'état ON à basse résistance à une tension d'environ +0.8 V et reviennent à l'état OFF pour la polarité opposée à environ 2.5 V.

De plus, l'électroformage n'est pas nécessairement demandé pour déclencher le premier cycle de commutation dans les conditions quasi-statiques. Il semble que la formation de lacunes d'oxygène comme première étape de l'électroformage se produise à une tension inférieure à la tension de commutation observée et que la tension de commutation exacte observée dans les conditions quasi-statiques soit fonction de la vitesse de balayage de la tension.

Interprétation du comportement électronique

La nature générale de la courbe de commutation est continue, ce qui indique un mouvement continu des ions d'oxygène. Le mouvement des lacunes d'oxygène et le piégeage/dépiégeage des électrons déterminent l'activité de commutation bipolaire dans les matériaux d'oxyde. Par différents moyens tels que le saut entre des sites adjacents sous l'influence du champ électrique, le déplacement le long d'une dislocation, des joints de grains, des surfaces, des interfaces, etc. les vacances d'oxygène peuvent se déplacer dans l'échantillon. Un certain nombre de processus tels que l'émission de Poole-Frenkel, la conduction limitée par la charge d'espace (CLCE) et l'effet tunnel assisté par piège (TAT) ont été établis comme des canaux par lesquels les électrons peuvent être piégés/détachés. Le mécanisme de la conduction de charge dans l'oxyde diélectrique est largement classé en deux catégories et cela dépend des propriétés du diélectrique (limité par la masse) et de l'interface entre le diélectrique et les électrodes (limité par l'interface/électrode) [25]. Pour les films d'une épaisseur supérieure à 10 nm, l'émission Schottky sera le mécanisme de limitation d'interface le plus probable. Pour une émission Schottky, le tracé de ln (J/T2) en fonction de E1/2 doit être linéaire. De plus, lorsque le milieu contient des pièges, tels que des vacances d'oxygène, il y aura une transition des porteurs de charge dans la bande de conduction une fois que le matériau est activé thermiquement. Un tel phénomène est appelé l'émission de Poole-Frenkel (PF). Pour ce type de conduction, le tracé de Ln(J/E) en fonction de E1/2 doit être linéaire. La conduction limitée par la charge d'espace (CLCE) se produit lorsque la formation d'une région de charge d'espace entre l'électrode et l'interface métallique empêche le flux de charges dans le diélectrique. Pour le mécanisme CLCE, le tracé de J par rapport à V2 est linéaire. Pour distinguer les différents mécanismes de conduction, il est nécessaire d'identifier les valeurs correctes de la constante diélectrique ε_r déduites de l'ajustement et de les comparer à la valeur attendue. Par exemple, les valeurs rapportées de ε_r pour les films WO_3 sont dans la gamme ~3-6 [94] [95]. Le tableau 4.1 montre les différents paramètres dérivés. Le modèle CLCE donne ε_r~ 9 et 4 pour les cycles positifs et négatifs,

respectivement. L'ajustement linéaire avec le mécanisme de Schottky donne une valeur de ~ 5 pour la constante diélectrique dans le cycle positif et ~ 6 dans le cycle négatif [96].

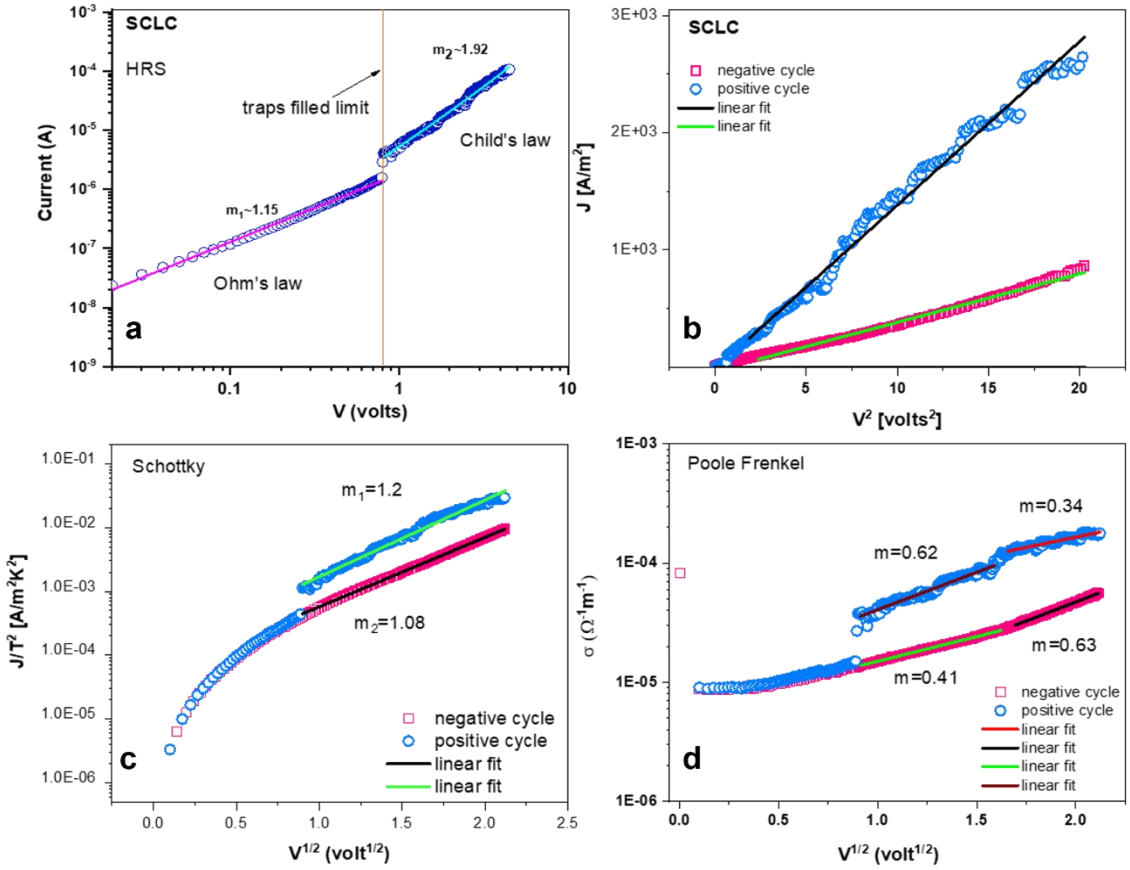

Figure 4.5: Ajustement des caractéristiques I-V aux différents modèles de conduction (a et b) CLCE (c) Schottky et (d) Poole-Frenkel.

Paramètres	cycle SCLE		Cycle Schottky		Cycle Poole Frenkel	
Unités SI	+ve	-ve	+ ve	-ve	+ ve	- ve
θ rapport porteurs libres / porteurs totaux	10^{-3}	10^{-3}	-	-	-	-
ε_r Permittivité diélectrique	9	4	5	6	-	-
µ (cm^2/Vs) Mobilité des porteurs	12	12	-	-	12	12

Tableau 4.1: Paramètres d'ajustement pour divers mécanismes de conduction dans les cellules PEDOT:PSS/WO_3/PEDOT:PSS

Endurance et rétention

Pendant que la rétention est la mesure de la capacité d'un dispositif à conserver l'information stockée sur une période de temps, l'endurance fait référence à la performance durable du dispositif sur des cycles de commutation bipolaire. Pour évaluer l'endurance des dispositifs, les résistances du LRS (ON) et du HRS (OFF) sur une seule barre transversale à une tension de lecture de 0.5 V sur 6000 cycles en utilisant une séquence de commutation pulsée avec des impulsions d'écriture/effacement avec une amplitude de 3.5V/-3.5V. Les états HRS et LRS ont pu être distingués jusqu'à 22 heures, lorsque l'état de faible résistance ne peut plus être atteint. Pour un des échantillons du même lot, les états ON/OFF restent stables jusqu'à 6000 cycles.

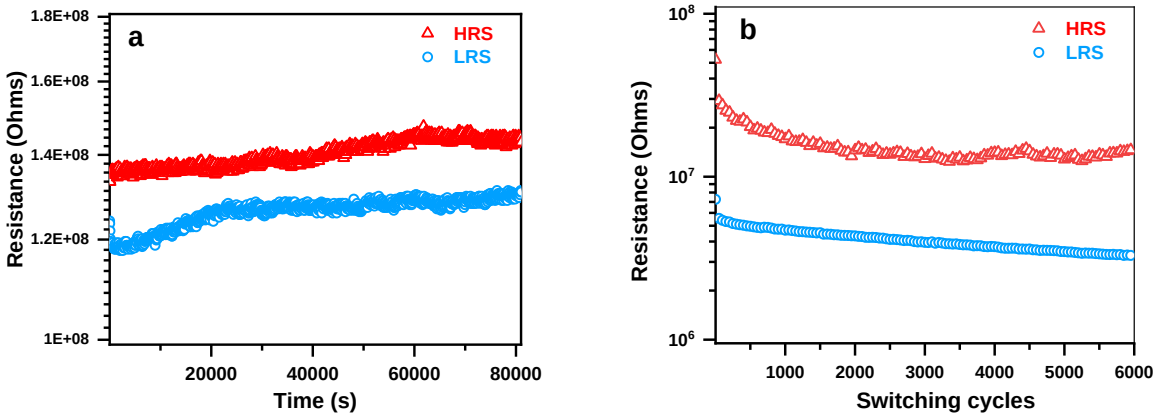

Figure 4.6: (a) Comportement de rétention de la cellule mémoire PEDOT:PSS/WO3/PEDOT:PSS (b) Réponse de commutation résistive induite par impulsion sur des cycles de commutation bipolaires répétitifs.

Cellules de mémoire PEDOT:PSS/ZnO/PEDOT:PSS

Analogue au dispositif à base de WO_3 décrit dans la section 2.1, la couche isolante dans l'élément de mémoire MIM consiste maintenant en ZnO pris en sandwich entre des électrodes de

PEDOT:PSS. Le procédé de dépôt à la demande, les paramètres et le substrat restent identiques pour des raisons de comparabilité.

Processus de fabrication

Tous les paramètres sont identiques à ceux de la fabrication avec l'encre WO_3, à l'exception des points suivants : L'isolant ZnO est maintenant imprimé avec un espacement des gouttes de 10 µm en quatre couches pour permettre une commutation stable à des tensions pratiques.

Caractérisation électrique

Les sondes en tungstène sont directement mises en contact avec les électrodes inférieure et supérieure du PEDOT:PSS. Les courbes I-V sont réalisées en utilisant un balayage de tension de +5 V à -5 V. Un schéma du système PEDOT : PSS/ZnO/PEDOT:PSS est illustré à la figure 2.6a. La figure 2.6b montre la caractéristique courant-tension I(V) du dispositif de mémoire, ainsi qu'un encart de la caractéristique I(V) sur une échelle semi-logarithmique. Des impulsions de tension de +5 V à -5 V ont été appliquées à l'électrode supérieure. Le comportement de commutation des cellules de mémoire révèle la présence d'un processus de commutation multiniveau dans la direction de balayage positive de HRS à LRS, le LRS continuant dans la direction de balayage négative. Un événement de commutation unique d'un LRS vers un HRS est détecté dans la direction de balayage négative, démontrant un comportement de commutation bipolaire non volatile. La tension de réglage estimée V_{set} est ≈ 0.7 V, tandis que la tension de réinitialisation V_{reset} ≈ 3.5 V dans ce cas. Le changement de résistance le plus élevé pour un balayage commençant dans la direction positive se produit à environ 0.7 V, comme on peut le voir dans l'encart de la figure 4.10b. Bien qu'une conception symétrique des électrodes puisse impliquer une courbe de commutation symétrique, certains rapports indiquent que l'électroformage implicite pendant le cycle de commutation initial provoque une asymétrie [105].

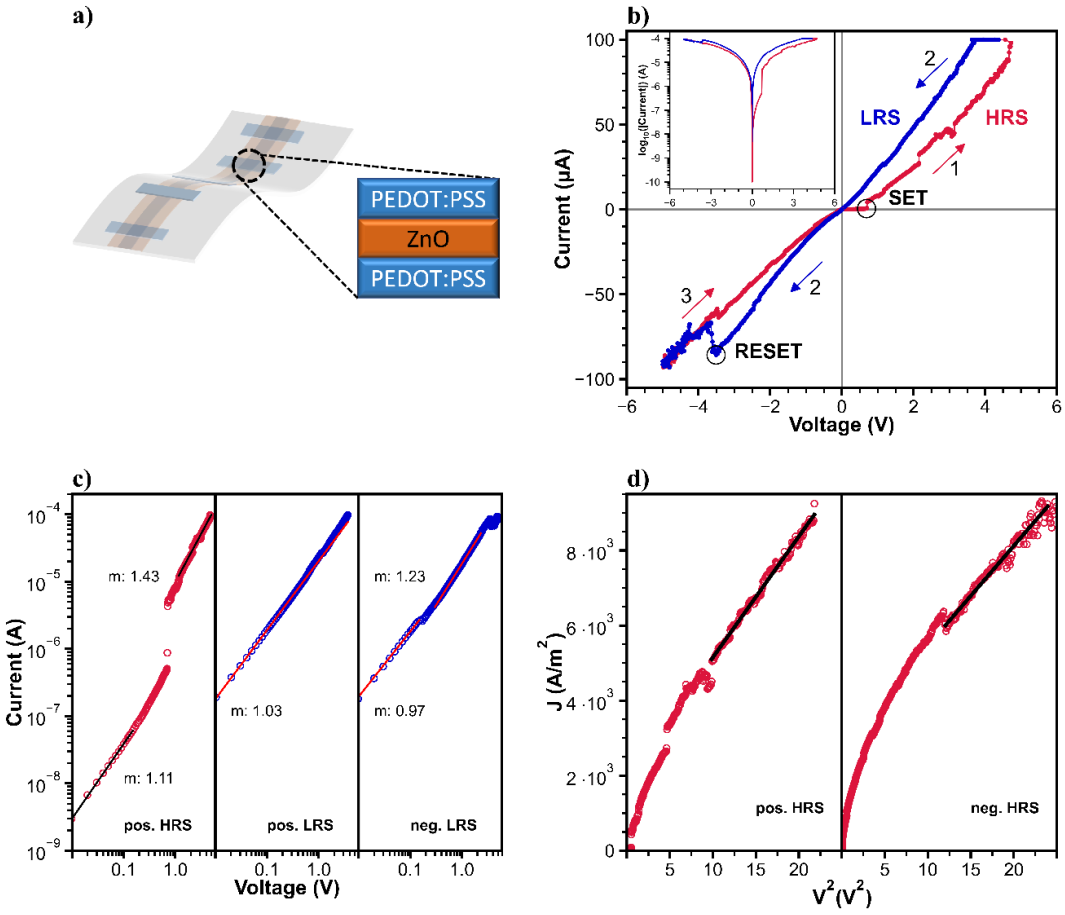

Figure 4.10 : (a) Schéma du système PEDOT : PSS/ZnO/PEDOT : PSS, (b) Caractéristiques courant-tension de la cellule de mémoire correspondante en mode de balayage DC, (c) Données expérimentales (symboles) et résultats de l'ajustement linéaire (solide) du HRS/LRS positif et du LRS négatif pour la courbe I(V) correspondante à l'échelle log-log pour déterminer le mécanisme de conduction, (d) Tracé d'ajustement CLCE du HRS positif et négatif pour la plage de tension appliquée élevée[106].

Pour les HRS positifs et négatifs, la conductivité σ peut être déterminée en utilisant les dépendances géométriques et la valeur de résistance la plus faible. En outre, la limite de remplissage des pièges pour les SRH positifs et négatifs ayant été dépassée, θ cette estimation sera exclue. Les paramètres d'ajustement du CLCE et ceux de la densité et de la mobilité des porteurs de charges libres ont ensuite été utilisés pour déterminer la permittivité diélectrique, comme indiqué dans le tableau 2.2 : Résumé des propriétés du SRH.

	$\boldsymbol{\varepsilon_r}$	$\boldsymbol{\mu}$ ($cm^2V^{-1}s^{-1}$)	$\boldsymbol{n_0}$ (cm^{-3})
HRS positive	8.53	$6.9 \cdot 10^{-6}$	10^{18}
HRS négative	7.50	$6.4 \cdot 10^{-6}$	10^{18}

Tableau 4.2: Résumé des propriétés de HRS

Bien que les valeurs de μ soient relativement faibles [108], la valeur publiée de la densité de porteurs de charge libre de $n_0 \approx 10^{18}$ cm^{-3} a été utilisée pour l'estimation de la permittivité diélectrique [110]. La valeur ε_r calculée est en bon accord avec la valeur de 8.3 du SRH positif par rapport au SRH négatif, dont la valeur ε_r est plus petite. La rupture du filament conducteur entraîne le déplacement des lacunes d'oxygène dans le sens inverse du flux d'électrons, ce qui explique cette divergence.

Endurance et rétention

Cette étude a été réalisée de manière similaire au dispositif basé sur le WO_3. Le rapport entre les phases HRS et LRS est d'environ 5 pendant le cycle et reste constant pendant 10^4 cycles. Une polarisation par impulsion de 5 V pendant 0.5 s a été utilisée pour les mesures de rétention, ce qui a permis d'obtenir un rapport constant entre les phases HRS et LRS jusqu'à $2{,}5x10^5$ s, comme le montre la figure 4.12b.

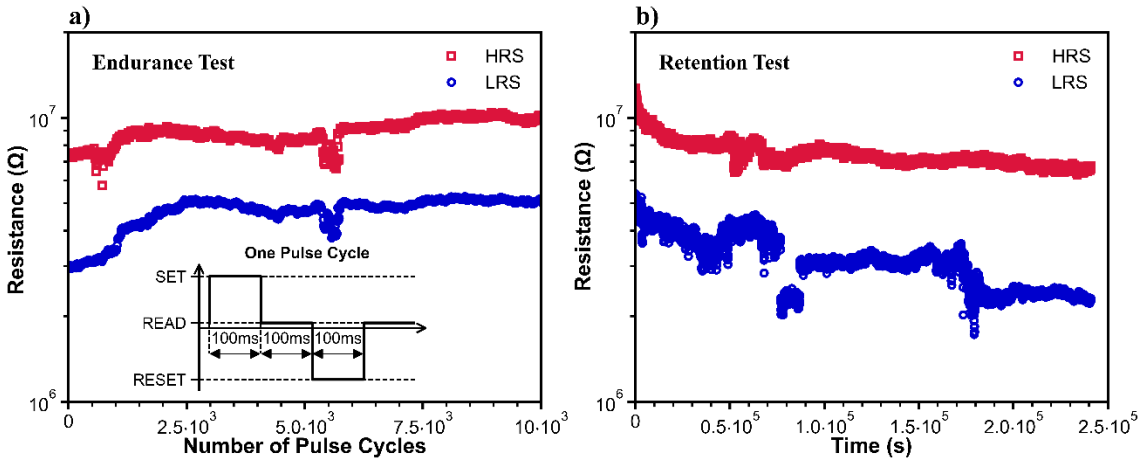

Figure 4.12: (a) Endurance mesurée pour 10^4 cycles d'impulsions. La figure en médaillon indique les séquences d'impulsions appliquées avec les paramètres de mesure utilisés (b) Caractéristiques de rétention de la cellule mémoire transparente flexible PEDOT : PSS/ZnO/PEDOT:PSS à température ambiante.

Fatigue induite par la flexion pour la cellule PEDOT:PSS/ZnO/PEDOT:PSS

Comme pour les cellules à base de WO_3, 700 cycles de flexion ont été effectués avec un rayon de flexion de 3,1 mm. Comme le montre la figure 2.9, la résistance augmente régulièrement, à partir de 31,8 kΩ, jusqu'à atteindre un point où la conduction le long de l'électrode PEDOT : PSS s'interrompt, car il s'agit d'un processus par étapes.

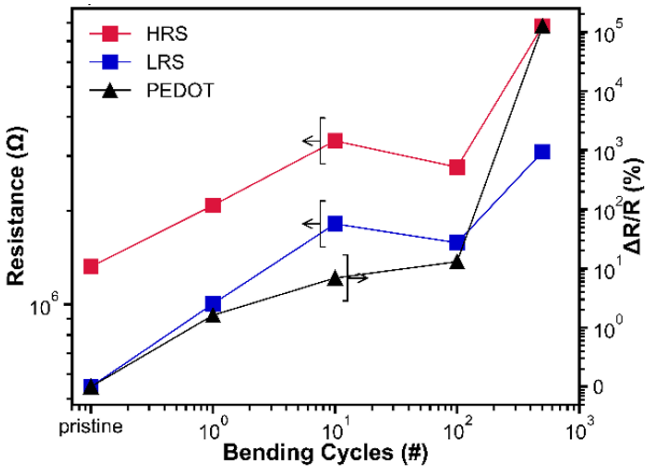

Figure 4.13: Évaluation des performances de flexion de la mémoire. Les carrés (en couleurs) représentent les valeurs de résistance pour HRS et LRS mesurées à 0.5V. Les triangles indiquent la variation relative de la résistance mesurée pour une électrode PEDOT:PSS. Les flèches sur la figure indiquent l'axe Y correspondant.

Comparaison entre WO_3 et ZnO

La comparaison directe du WO_3 et du ZnO doit inclure une variété de paramètres, qui ne sont pas tous nécessairement liés aux performances des dispositifs décrits ci-dessus. Le potentiel d'un matériau pour les applications ReRAM imprimées est également lié au coût de l'encre, à sa manipulation, à sa toxicité et à sa capacité de recyclage.

En ce qui concerne ce dernier point, il convient de noter que le substrat polymère apporte de loin la plus grande quantité de matériaux aux dispositifs, suivi par les électrodes polymères et seulement ensuite par le matériau de changement de valence à base d'oxyde. Ainsi, en termes d'économie circulaire, les dispositifs étudiés sont en grande partie des articles en polymère et seront traités comme tels.

En termes de coûts, les dispositifs décrits ci-dessus présentent l'avantage de ne nécessiter que deux encres différentes, ce qui réduit la complexité de la configuration d'impression et évite les encres à base de métaux nobles.

Cependant, à l'heure actuelle, les coûts des encres sont encore principalement déterminés par les coûts de recherche et de développement et la production de nanoparticules à distribution de taille étroite, ce qui maintient l'avantage des coûts des matériaux par rapport aux autres encres à un niveau relativement faible.

Les deux encres permettent un processus de fabrication sans frittage avec une température maximale de 60 degrés Celsius associée au dépôt des électrodes supérieure et inférieure. Cela représente un avantage substantiel par rapport aux encres à nanoparticules métalliques dans le CBRAM.

La comparaison directe entre WO_3 et ZnO doit être faite dans le contexte de la commutation par changement de valence pure. Les rapports antérieurs dans la littérature sur la commutation résistive dans les dispositifs imprimés en ZnO et jusqu'à présent, tout ce qui a été publié sur les dispositifs à base de TiO_2, concerne le CBRAM, de sorte que les rapports ON/OFF précédemment rapportés de trois ordres de grandeur et plus ne doivent pas être pris en considération ici.

	PEDOT:PSS/WO_3/PEDOT:PSS	PEDOT:PSS/ZnO/PEDOT:PSS
Résistivité OFF (Ωcm)	5.19×10^6	3.51×10^7
Rapport ON/OFF à la tension de lecture	5.70	48.13
Temps de rétention (s)	80×10^3	2.5×10^5
Endurance (cycles)	6000	10 000
Transmission (longueurs d'onde visibles)	> 53%	> 86%
Cycles de flexion avant rupture	>700	>700

Tableau 4.3: Résumé comparatif

Quant à la résistivité OFF, nous voyons que pour le cas de ZnO, nous obtenons des valeurs qui sont $3,51X10^7$ Ωcm. Pour WO_3, la résistivité OFF est $5,19X10^6$ Ωcm, ce qui indique la présence de courants de fuite. La résistivité quelque peu plus faible par rapport au bulk (massif) est attribuée à une grande quantité de joints de grains avec des propriétés électroniques qui s'écartent substantiellement du bulk [113][114].

Comme la résistance ON dépend essentiellement de la nature du filament, de ses propriétés électroniques et de sa géométrie, les barres d'erreur sur ces valeurs sont plus importantes. Une incertitude provient de la vitesse à laquelle le circuit de conformité du courant est capable de réagir, ce qui laisse des incertitudes sur la taille du filament.

Concernant la rétention, la résistance à la fatigue et la transparence optique, le ZnO semble être supérieur au WO_3 dans tous les aspects. En rappelant que la couche de ZnO est plus fine que la couche de WO_3, ce qui affecte la transmittance optique via la loi de Lambert-Beer, il est possible d'améliorer la transparence du WO_3. Cela se ferait toutefois au détriment d'une résistance à l'extinction plus faible. Le nombre de cycles de commutation possibles est également plus important dans le ZnO (10 000) que dans le WO_3 (6 000) et, bien que les deux valeurs soient très certainement loin de l'optimum qui pourrait être atteint pour des impulsions de commutation encore plus courtes, il existe une tendance claire en faveur du ZnO dans des conditions similaires.

En ce qui concerne les expériences de flexion, le nombre de cycles de flexion n'a pas été limité par l'une ou l'autre des deux couches d'oxyde ; dans les deux cas, les dispositifs ont échoué en raison de la formation de fissures dans les électrodes polymères et apparemment, aucun des deux matériaux n'a eu d'effet tangible sur les propriétés mécaniques des électrodes. Dans l'ensemble, l'utilisation de ZnO fournit des résultats supérieurs en comparaison directe avec des dispositifs similaires basés sur WO_3, qui reste cependant un choix de matériau approprié.